Motionnet

G9004

(CPU emulation device)

User's Manual

NPM Nippon Pulse Motor Co., Ltd.

[Preface]

Thank you for considering our super high-speed serial communicator LSI, the "G9000."
To learn how to use the G9000 series device, read this manual and "G9001/G9002" user's manual to become familiar with the product.
The handling precautions for installing this LSI are described at the end of this manual. Make sure to read them before installing the LSI.

[What the Motionnet is]

As a next generation communication system, the Motionnet can construct faster, more volume large scale, wire saving systems than the conventional T-NET systems (conventional LSI product to construct serial communication system by NPM). Further, it has data communication function, which the T-NET does not have, so that the Motionnet can control data control devices such as in the PCL series (pulse train generation LSI made by NPM).

The Motionnet system consists of one center device connected to a CPU bus, and maximum 64 local devices, and they are connected by using cables of two or three conductive cores.

[Cautions]

(1) Copying all or any part of this manual without written approval is prohibited.

(2) The specifications of this LSI may be changed to improve performance or quality without prior notice.

(3) Although this manual was produced with the utmost care, if you find any points that are unclear, wrong, or have inadequate descriptions, please let us know.

(4) We are not responsible for any results that occur from using this LSI, regardless of item (3) above.

INDEX

1. Outline 1

2. Features 1

3. General specifications 1
   3-1. Communication system specifications 1
   3-2. Specifications of the CPU emulation device (G9004) 1

4. Hardware description 3
   4-1. A list of terminals (QFP-80) 3
   4-2. Terminal assignment drawings 5
   4-3. Entire block diagram 6

5. Functions of terminals 7
   5-1. CLK 7
   5-2. RST 7
   5-3. DN0 to 5 7
   5-4. DNSM 7
   5-5. DNSO 8
   5-6. SPD0, SPD1 8
   5-7. TUD 8
   5-8. TMD 8
   5-9. TOUT 8
   5-10. SO 8
   5-11. SOEH, SOEL 8
   5-12. SOEI 9
   5-13. SI 9
   5-14. MRER 9
   5-15. MSEL 9
   5-16. BRK 9
   5-17. MOD 9
   5-18. LCK0 to 1 9
   5-19. LCLK 9
   5-20. LIF0 to 1 10
   5-21. LRST 10
   5-22. LIFB 10
   5-23. LA0 to LA5 10
   5-24. LCS 10
   5-25. LWR 10
   5-26. LRD 10
   5-27. LWRQ 11
   5-28. LIRQ 11
   5-29. LD0 to LD7 11
   5-30. LD8 to LD15 11
   5-31. LWT0 and LWT1 11
   5-32. CKSL 12
   5-33. VDD, GND 12

6. Status information and setting operation information for the G9004 13

7. Message communication mode (MOD = LOW) 15
   7-1. Terminals for use by a local CPU 15
   7-2. I/O map for the local CPU 15
   7-3. Command and status information that can be used by a local CPU 16
   7-4. Information command for the central device (G9001) 17
   7-5. Message communication procedure 18

8. CPU emulation mode (MOD = H) 20
8-1. Terminals on the G9004 20
8-2. Control method for using a central device (G9001) 21
8-3. Emulation timing 30

9. Connection examples and recommended environment 35
9-1. Example of a connection to a CPU using the CPU message communication mode (MOD = L) 35
9-2. Access timing when the CPU message communication mode is selected (MOD = L) 40
9-3. Connection to peripheral LSIs when the CPU emulation mode is selected 42
9-4. Connections to a serial communication line 44
9-5. A connection example of a level shifter 46
9-6. Complete configuration 47
9-7. Recommended environment 48

10. Center device (G9001) 51
10-1. Program example of CPU emulation mode 52

11. Electrical characteristics 56
11-1. Absolute maximum ratings 56
11-2. Recommended operating conditions 56
11-3. DC characteristics 56
11-4. AC characteristics 57
11-5. Timing of CPU message communication mode 58
11-6. Timing when CPU emulation is selected 62

12. External dimensions 67

13. Handling precautions 68
13-1. Design precautions 68
13-2. Precautions for transporting and storing LSIs 68
13-3. Precautions for mounting 69
13-4. Other precautions 69

1. Outline

This LSI is a CPU emulation device (G9004). This LSI can be connected to our Motionnet and perform data communications with a center device (G9001).
Either of the following two operation modes can be selected from a terminal.

1) CPU emulation mode
In this mode, the G9004 emulates CPU terminal signals using data communicated from the center device (G9001). Although the communication format from the central device is limited, this LSI outputs signals identical to those from CPU terminals. Therefore it can control various LSIs that are normally connected to a CPU.

2) Message communication mode
One word (16 bits) is reserved by the system in this mode, which is used for communication (the data commands and formats are specified). The user can use the remaining 127 words to communicate data.
The format for the message data is not specified, which means that this LSI can communicate freely with almost any CPU that is connected to the central device and to this LSI.

2. Features

- Compatible with our Motionnet.
- Can control various CPU support LSIs using data communications.
- A maximum of 256 bytes of data can be communicated in one sentence.
- A maximum of 64 devices can be connected using one line.
- It has a safety design using a communication failure detection circuit (contains a watchdog timer).
- Powered from just 3.3 VDC.

3. General specifications

3-1. Communication system specifications

Item	Description
Reference clock	40 MHz or 80 MHz
Communication speed	2.5 M, 5 M, 10 M, or 20 Mbps
Communication sign	NRZ sign
Communication protocol	NPM original method
Communication method	Half-duplex communication
Communication I/F	RS-485 or pulse transfer
Connection method	Multi-drop connection
Number of local devices	64 devices max.
Cyclic communication cycle when 20 Mbps	When using 8 local devices (IN: 128 points, OUT: 128 points) --- 0.12 msec. When using 16 local devices (IN: 256 points, OUT:256 points) --- 0.24 msec. When using 32 local devices (IN: 512 points, OUT: 512 points) --- 0.49 msec. When using 64 local devices (IN: 1024 points, OUT: 1024 points) --- 0.97 msec. Note: The communication cycle will be extended dependant upon data communication.

3-2. Specifications of the CPU emulation device (G9004)

Item		Description
CPU emulation mode		
	Communication sentence length	1 to 128 words/frame (1 word = 16 bits)
	Data buffer size	128 words
	Data communication time	When communicating 5 words (write to one register in the PCL): 21.7 µs
	Data transfer method	Status: Cyclic transfer, Data: Transient transfer
	Control address space	64 bytes
	CPU interface	8-bit I/F --- Z80, 6809 etc. 16-bit I/F --- 8086, H8, 68000 etc.
Message communication mode		
	Communication sentence length	1 to 128 words/frame (1 word = 16 bits)
	Data buffer size	128 words (1 word: reserved for the system, 127 words: Message data)
	Data communication time	When communicating 128 words: 169.3 µs
	Data transfer system	Status: Cyclic transfer Data communication: Transient transfer
	CPU interface	8-bit I/F --- Z80, 6809 etc. 16-bit I/F --- 8086, H8, 68000 etc.
Others		
	Package	80 pin QFP (mold size: 12 x 12 x 1.4 mm)
	Power supply	3.3 V±10%
	Storage temperature range	-65 to +150℃
	Operating temperature range	-40 to +85℃

4. Hardware description

4-1. A list of terminals (QFP-80)

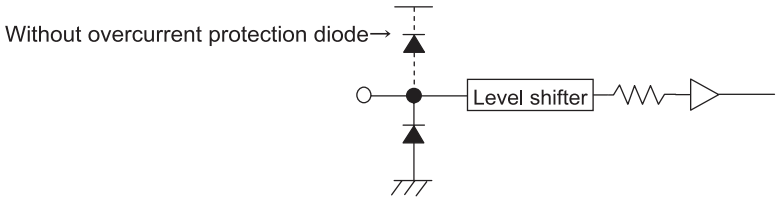
No.	Signal name	I/O	Logic	Description	5V Interface
1	MOD	I		Select operation mode (L: Message communication, H: CPU emulation)	Available
2	TUD	I		Set operation when outputting watchdog timer	Available
3	TMD	I		Select watchdog timer	Available
4	LCK0	I		Division rate of local bus control clock (LCLK): 0	Available
5	LCK1	I		Division rate of local bus control clock (LCLK): 1	Available
6	LWT0	I	Positive	Interval time of local bus: 0	Available
7	LWT1	I	Positive	Interval time of local bus: 1	Available
A1	LIF0	I		I/F mode setting bit 0	Available
9	LIF1	I		I/F mode setting bit 1	Available
10	VDD	I		+3.3 V power input	
11	LCS	I/O	Negative	Chip selection for local bus	Available
12	LWR	I/O	Negative	Write signal for local bus	Available
13	LRD	I/O	Negative	Read signal for local bus	Available
14	LA0	I/O	Positive	Address for local bus: 0	Available
15	GND	I		GND	
16	LA1	I/O	Positive	Address for local bus: 1	Available
17	LA2	I/O	Positive	Address for local bus: 2	Available
18	LA3	I/O	Positive	Address for local bus: 3	Available
19	LA4	I/O	Positive	Address for local bus: 4	Available
20	LA5	I/O	Positive	Address for local bus: 5	Available
21	VDD	I		+3.3 V power input	
22	LD0	B	Positive	Data for local bus: 0	Available
23	LD1	B	Positive	Data for local bus: 1	Available
24	LD2	B	Positive	Data for local bus: 2	Available
25	LD3	B	Positive	Data for local bus: 3	Available
26	GND	I		GND	
27	LD4	B	Positive	Data for local bus: 4	Available
28	LD5	B	Positive	Data for local bus: 5	Available
29	LD6	B	Positive	Data for local bus: 6	Available
30	LD7	B	Positive	Data for local bus: 7	Available
31	VDD	I		+3.3 V power input	
32	LD8	B	Positive	Data for local bus: 8	Available
33	LD9	B	Positive	Data for local bus: 9	Available
34	LD10	B	Positive	Data for local bus: 10	Available
35	LD11	B	Positive	Data for local bus: 11	Available
36	GND	I		+GND	
37	LD12	B	Positive	Data for local bus: 12	Available
38	LD13	B	Positive	Data for local bus: 13	Available
39	LD14	B	Positive	Data for local bus: 14	Available
40	LD15	B	Positive	Data for local bus: 15	Available
41	VDD	I		+3.3 V power input	
42	LWRQ	O/I	Negative	Wait request for local bus	Available
43	LIRQ	O/I	Negative	Interrupt request for local bus	Available
44	LIFB	O	Negative	Busy interface for local bus	Available
45	LRST	O	Negative	Reset for local bus	Available
46	GND	I		GND	
47	LCLK	O		Local bus control block	

No.	Signal name	I/O	Logic	Description	5V Interface
48	MRER	O	Negative	When a communication error is received, this signal becomes L level for a rated interval.	Available
49	MSEL	O	Negative	When sending data to this chip, this signal becomes L level for a rated interval.	Available
50	VDD	I		+3.3 V power input	
51	SOEH	O	Positive	Enable serial output	
52	SOEL	O	Negative	Enable serial output	
53	SO	O	Positive	Serial output	
54	TOUT	O	Negative	Watchdog timer output	Available
55	DNSO	O	Negative	Serial output of device number for next chip	Available
56	GND	I		GND	
57	BRK	I	Positive	Break frame send request	Available
58	SPD0	I		Communication speed: 0	Available
59	SPD1	I		Communication speed: 1	Available
60	CKSL	I		Clock rate selection (L: 40 MHz, H: 80 MHz)	Available
61	DNSM	I		Device number selection mode	Available
62	DN0	I	Negative	Device number bit 0 (common with serial input)	Available
63	DN1	I	Negative	Device number bit 1	Available
64	DN2	I	Negative	Device number bit 2	Available
65	DN3	I	Negative	Device number bit 3	Available
66	DN4	I	Negative	Device number bit 4	Available
67	DN5	I	Negative	Device number bit 5	Available
68	VDD	I		+3.3 V power input	
69	SI	I	Positive	Serial input	
70	SOEI	I	Positive	Enable serial output	
71	GND	I		GND	
72	CLK	I		Reference clock	
73	VDD	I		+3.3 V power input	
74	RST	I	Negative	Reset	
75	GND	I		GND	
76	GND	I		GND	
77	VDD	I		+3.3 V power input	
78	GND	I		GND	
79	GND	I		GND	
80	GND	I		GND	

Note 1: In the "I/O" column, each pin can be set for input or output using the operation mode (MOD). In the "I/O" column, "I" refers to input, "O" refers to output and "B" refers to bi-directional.

Note 2: As for the terminals with "available" in the 5V interface column, note the following.

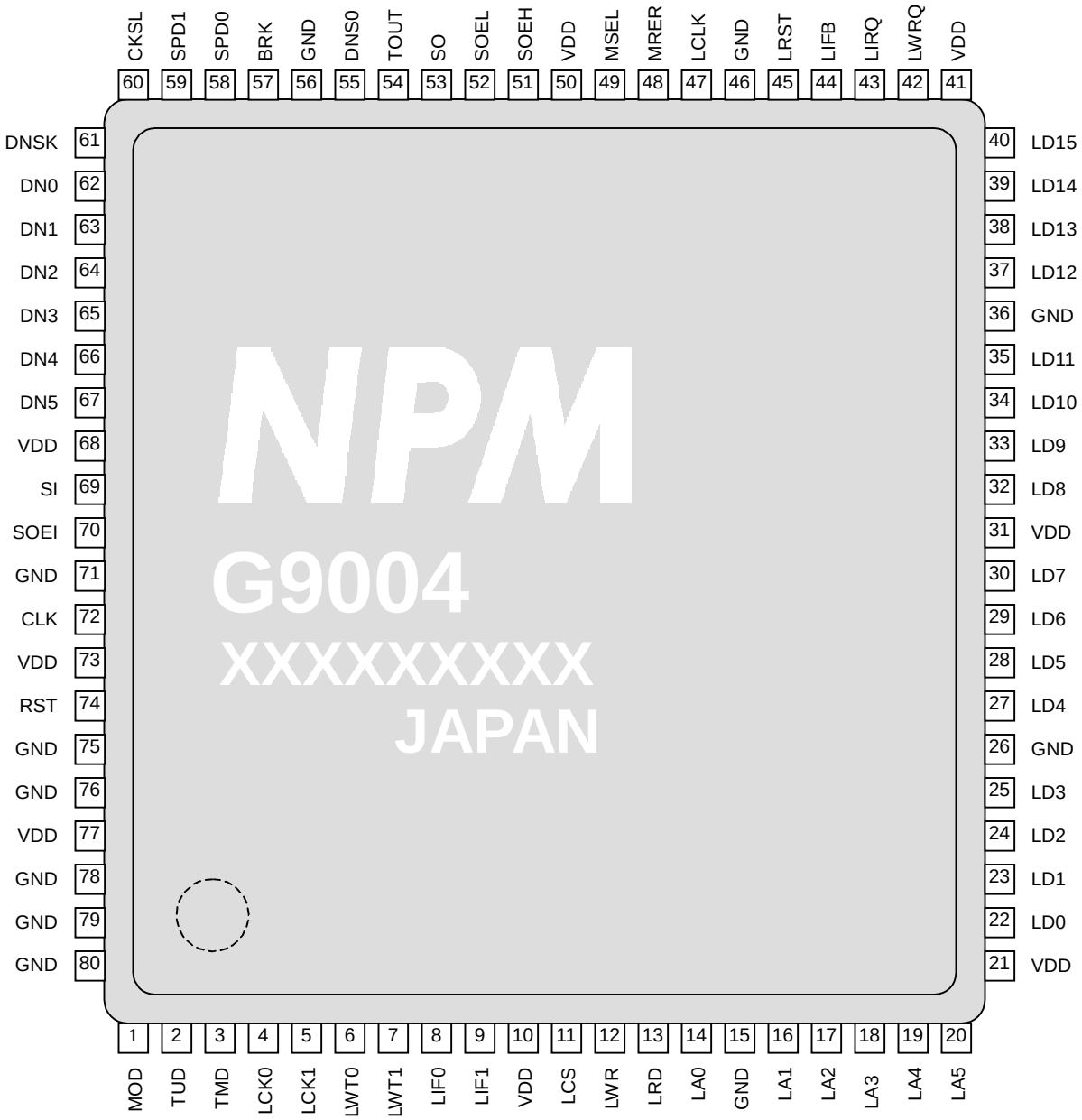
* These terminals can be input 5 V level signal. These are deleted diodes for overcurrent protection on 3.3 V lines. If over voltage may possibly be charged due to reflection, linking, or inductive noise, we recommend inserting a diode for overcurrent protection.



* Outputs from 5V devices can be connected to the center device as far as these are TTL level. (Even when a signal is pulled up to 5V, the output level will be less than 3.3 V.) However, CMOS level signals cannot be connected.

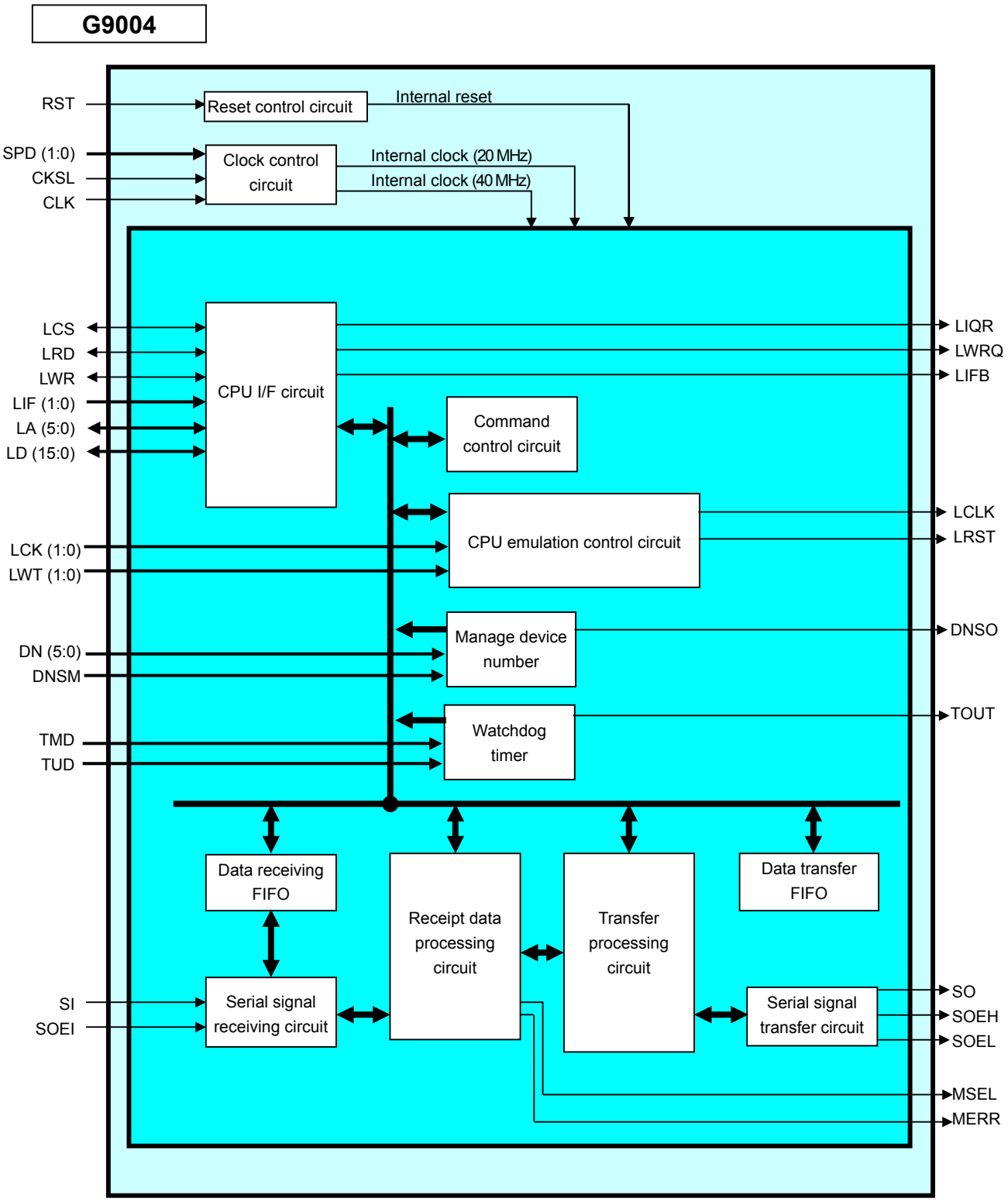
* On the CPU bus interface, pull up of a 5 V level is possible for stabilizing bus lines (prevent floating). Use 10 k-ohm or larger capacity pull up resistors.

4-2. Terminal assignment drawings



Note: Locate each pin number from the markings on the chip.
As shown in the figure above, pin number 1 is at the lower left of the NPM logo mark.

4-3. Entire block diagram



5. Functions of terminals

5-1. CLK

This is an input terminal of the reference clock. By setting of the CKSL terminal, either of the following clock rate signals can be connected.

CKSL = L: 40 MHz
CKSL = H: 80 MHz

By selecting either of these clock rates, the serial communication transfer rate does not change. This clock rate selection affects communication precision.
For a small-scale serial communication and transfer rate below 10 Mbps, use of the center device with 40 MHz does not give any restriction.
With 20 Mbps transfer speed; however, longer communication lines or a large number of connected local devices may deteriorate communication precision due to collapse of signals on the circuit. This deterioration of communication quality can be corrected inside the LSI, if the deterioration level is not much. In order to improve correction precision; however, evenness of the clock duty is required. In other words, if the duty is ideal (50:50), the capacity to correct collapse of the signals in the communication lines can be improved. On the contrary, if the duty is not ideal, the center device cannot cope with collapses of the communication line.

As a result, if the duty is close to ideal, the center device can be used with 40 MHz. When connecting more than one oscillator, the duty will not be ideal. In this case, select 80 MHz. The central device divides the frequency inside and creates 40 MHz frequency.
If you do not want to 80 MHz frequency, you may prepare a separate 40 MHz oscillator for this LSI.

5-2. RST

This is an input terminal for a reset signal.
By inputting an L level signal, the central device is reset.
The RST line must be held LOW for at least 10 reference clock cycles.
After turning ON the power, a reset signal must be input before starting communication.

5-3. DN0 to 5

Input terminals for setting device address.
Since these terminals use negative logic, setting all the terminals to zero calls up device address "3FH."
There are two methods for entering a device address. Select the input method using the DNSM terminal.

5-4. DNSM

Select the input method for loading the device address.
1) When the DNSM = H
Input numeric values 0 to 3Fh with negative logic using DIP-SW etc. for DN0 to DN5 terminals.

2) When the DNSM = L
Input a DASO signal that is output by some other chip on the DN0 terminal on this device. When using this input method, this chip has an address equal to the other chip's address plus one.
When using this method, connect terminals DN1 to DN5 to GND.
When two sequential sets of serial data match, the data is taken to be a device address.

5-5. DNSO

The numeric equivalent of the address on DN0 to DN5 + 1 will be output after being converted into a serial bit stream.
Connect this output to another local device's DN0 terminal (make all the other DNSM terminals of that local device LOW), so that other devices can get the address and pass it along to the next data-sending device.

5-6. SPD0, SPD1

Specify communication speed with these terminals.
All of the devices on the communication line shall be set to the same speed.

SPD1	SPD0	Communication speed
L	L	2.5 Mbps
L	H	5 Mbps
H	L	10 Mbps
H	H	20 Mbps

5-7. TUD

A watchdog timer is included on the chip to assist in administration of the communication status.
When the data transmission interval from a central device to this device exceeds the set time, the watchdog timer times out.
This terminal is used to set output conditions when the watchdog timer times out.
When TUD = HIGH --- The LSI keeps its current status.
When the TUD = LOW --- The LSI is Reset.

5-8. TMD

Specify the time for the watchdog timer.
The watchdog timer is used to administer the communication status.
When the interval between data packets sent from a central device is longer than the specified interval, the watchdog timer times out (the timer restarts its count at the end of each data packet received from a central device). The time out may occur because of a problem on the communication circuit, such as disconnection, or simply because the central device has stopped communicating.
The time used by the watchdog timer varies with communication speed selected.

TMD terminal	Watchdog timer setting			
	20 Mbps	10 Mbps	5 Mbps	2.5 Mbps
L	5 ms	10 ms	20 ms	40 ms
H	20 ms	40 ms	80 ms	160 ms

5-9. TOUT

Once the watchdog timer has timed out, this terminal goes LOW.

5-10. SO

Serial output signal for communication. (Positive logic, tri-state output)

5-11. SOEH, SOEL

Output enable signal for communication.
Difference between SOEH and SOEL is that only the logic is different.
When sending signals, SOEH will become H and SOEL will become L.

5-12. SOEI

When using more than one I/O device, connect the SOEH signal of the other I/O device to this terminal.
By being wire OR'ed with the output enable signal from this I/O device, the device outputs an enable signal to SOEH or SOEL.
When not used, connect to the GND.

5-13. SI

Serial input signal for communication. (Positive logic)

5-14. MRER

This is a monitor output to check communication quality.
When the center device receives an error frame such as a CRC error, the signal becomes L only for 128 cycles (3.2 μs) of the CLK.
By measuring the condition using the counter, you can check communication quality.

5-15. MSEL

Communication status monitor output.
When the I/O device receives a frame intended for this device and everything is normal (when communication MRER is OFF), this terminal goes LOW for exactly 128 CLK cycles (3.2 μs). This can be used to check the cyclic communication time.

5-16. BRK

By providing HIGH pulses that are longer than the specified interval, the I/O device will be made to wait for a break frame.
When the I/O device receives a break frame send request from a central device, it immediately sends a break frame.
A pulse at least 3200 μsec long is needed, in order to be seen as the BRK input pulse (positive logic).

5-17. MOD

Selects the operating mode for this IC.
MOD = L: Message communication mode
MOD= H: CPU emulation mode

5-18. LCK0 to 1

Selects the clock frequency (LCLK) for controlling a local bus.

LCK1	LCK 0	The clock frequency (LCLK)
L	L	2 MHz
L	H	4 MHz
H	L	10 MHz
H	H	20 MHz

When this IC is in CPU emulation mode, the speed of the emulation depends on the above setting. However, when the message communication mode is selected, only the LCLK output frequency will change, and the operation speed remains constant.

5-19. LCLK

Outputs a clock for controlling a local bus.
If needed, it can be used for an external circuit.

5-20. LIF0 to 1

Using these terminals, select the CPU interface specifications for the local bus.

LIF1	LIF 0	CPU-I/F interface
L	L	I/F-16 bit (2) (68000, etc)
L	H	I/F-16 bit (1) (8086, H8, etc)
H	L	I/F-8 bit (2) (6809, etc)
H	H	I/F-8 bit (1) (Z80, etc)

5-21. LRST

Output a reset signal for the local bus.
In any of the following cases, this signal goes LOW.

1) When a LOW is applied to the RST terminal.
2) When TUD is LOW, the watchdog timer has timed out (only effective during the first 32 cycles on LCLK).

The LRST terminal status can be changed by setting bit 1 of port 3 (See section 6 "Setting the status information and G9004 operation information.")
(When bit 1 = 0, LRST = HIGH. When bit 1 = 1, LRST = LOW.)

5-22. LIFB

Outputs an interface busy signal for the local bus.
Use this signal in the message communication mode when connecting to a CPU that does not have a wait control input terminal.
This terminal goes LOW when a command or data is sent from a CPU, or when the status is being read. When this LSI completes its internal processing, it goes HIGH. Make sure that this terminal is HIGH, and then you can access the LSI.
This terminal cannot be used in the CPU emulation mode.

5-23. LA0 to LA5

Address signals for the local bus. These will be either input or output terminals, depending on the mode selected.
In the CPU emulation mode, the device outputs address signals from terminals LA0 to LA5.
In the message communication mode, input address signals on LA0 and LA1. Pull LA2 to LA5 down to GND (5~10Kohm resistors).

5-24. LCS

This is a chip select signal for the local bus. It will be either an input or output terminal, depending on the mode selected.
In the CPU emulation mode, this device outputs a chip select signal for an external circuit.
In the message communication mode, you supply a chip select signal that will be used to access this LSI.

5-25. LWR

This terminal is used for a write signal for a local bus. It will be either an input or output terminal, depending on the mode selected.
In the CPU emulation mode, this terminal outputs a write signal for external circuit.
In the message communication mode, you supply a write signal in order to access this LSI.

5-26. LRD

This terminal is used for a read signal for a local bus. It will be either an input or output terminal, depending on the mode selected.
In the CPU emulation mode, this terminal outputs a read signal for an external circuit.
In the message communication mode, you supply a read signal in order to access this LSI.

5-27. LWRQ

This terminal is used for a wait request signal for a local bus. It will be either an input or output terminal, depending on the mode selected.
In the CPU emulation mode, you supply a wait request signal from an external circuit.
In the message communication mode, this terminal outputs a wait request signal when the device cannot be accessed.

5-28. LIRQ

This terminal is used for an interrupt request signal for a local bus. It will be either an input or output terminal, depending on the mode selected.
In the CPU emulation mode, you supply an interrupt request signal from an external circuit.
In the message communication mode, this terminal outputs an interrupt request signal from internal operations.

5-29. LD0 to LD7

These terminals are used for the low-byte signals of a local data bus. These are bi-directional terminals.

5-30. LD8 to LD15

These terminals are used for the high-byte signals of a local data bus. These are bi-directional terminals.
When using an 8-bit CPU interface, pull up these terminals to VDD (5 to 10 K-ohm resistors).

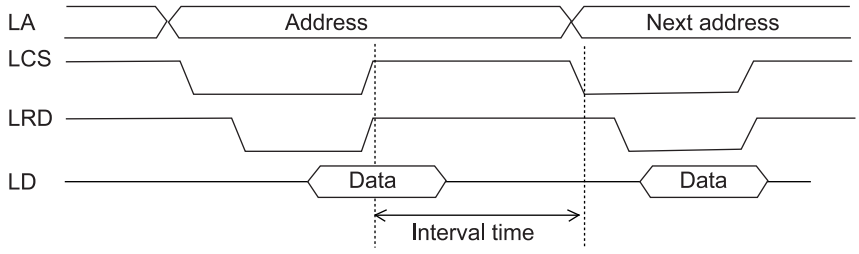
5-31.LWT0 and LWT1

These terminals are used to set the time interval between writing and reading to a local bus. Use these terminals only in the CPU emulation mode. These are not used in the message communication mode.

(T_{LCLK}: LCLK clock cycle)

LWT1	LWT0	Time interval
L	L	T_{LCLK}
L	H	$3xT_{LCLK}$
H	L	$5xT_{LCLK}$
H	H	$9xT_{LCLK}$

[An example of the reading procedure when using a 16-bit CPU interface (1)]



5-32.CKSL

Selects the clock specifications for the input on the CLK terminal.
When CKSL = L, supply a 40 MHz clock signal on the CLK terminal. The duty cycle should be approximately 50%.
If the duty cycle is too far away from 50%, the number of communication faults will increase.
When CKSL = H, the device uses the CLK signal input after dividing by 2 internally.
Therefore, the duty cycle will not have such a great influence. In this case, supply an 80 MHz clock signal.

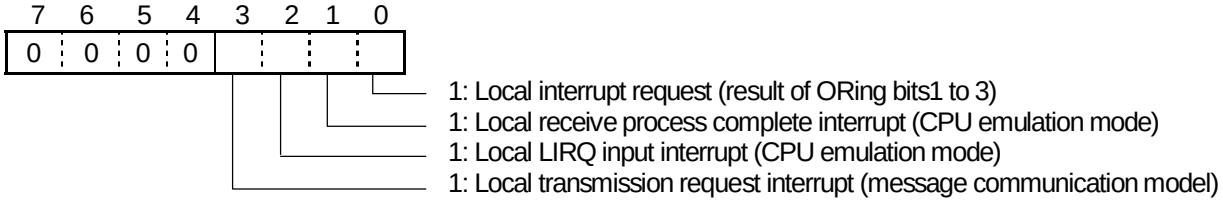
5-33.VDD, GND

Supply +3.3 VDC±10% for power on the VDD terminal.
Make sure to use all the terminals.

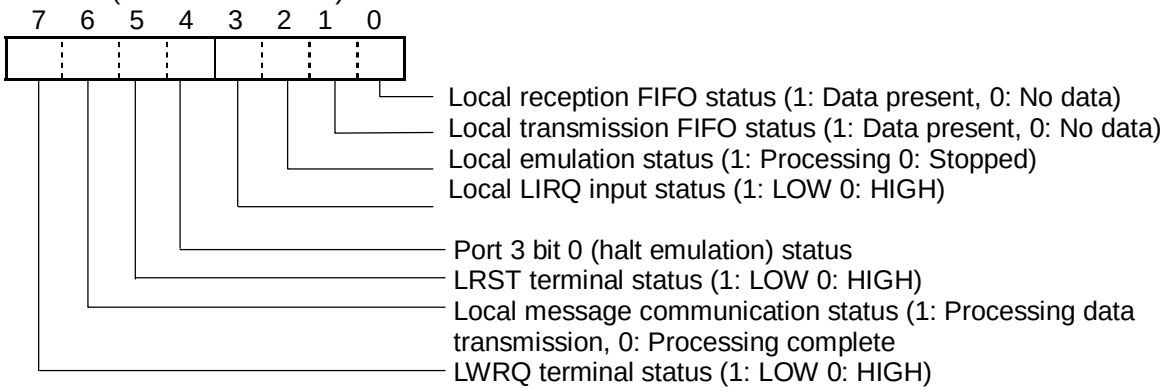
6. Status information and setting operation information for the G9004

During the I/O communication cycle and during data communication, the status register information (registers 0 to 2) is written to the port data area (ports 0 to 2) that corresponds to the device address in the central device.
When the operating information is written to the port data area (port 3) that corresponds to the central device's device address, it is passed along to the CPU emulation device (G9004) using the I/O communication cycle.

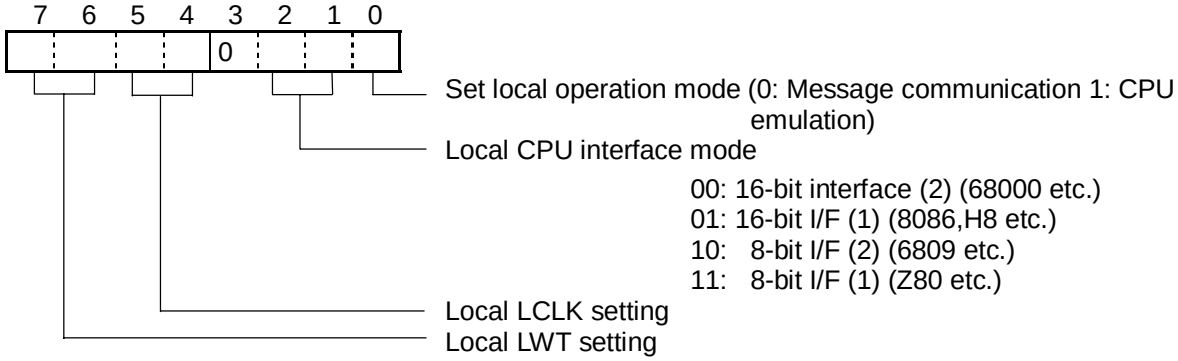
Status 0 (Interrupt information) <Port 0>


7 6 5 4 3 2 1 0
0 0 0 0
1: Local interrupt request (result of ORing bits1 to 3)
1: Local receive process complete interrupt (CPU emulation mode)
1: Local LIRQ input interrupt (CPU emulation mode)
1: Local transmission request interrupt (message communication model)

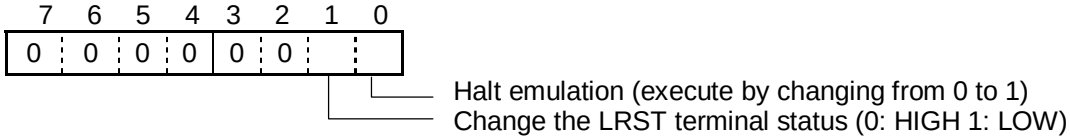
Status 1 (Status information) <Port 1>


7 6 5 4 3 2 1 0
Local reception FIFO status (1: Data present, 0: No data)
Local transmission FIFO status (1: Data present, 0: No data)
Local emulation status (1: Processing 0: Stopped)
Local LIRQ input status (1: LOW 0: HIGH)
Port 3 bit 0 (halt emulation) status
LRST terminal status (1: LOW 0: HIGH)
Local message communication status (1: Processing data transmission, 0: Processing complete
LWRQ terminal status (1: LOW 0: HIGH)

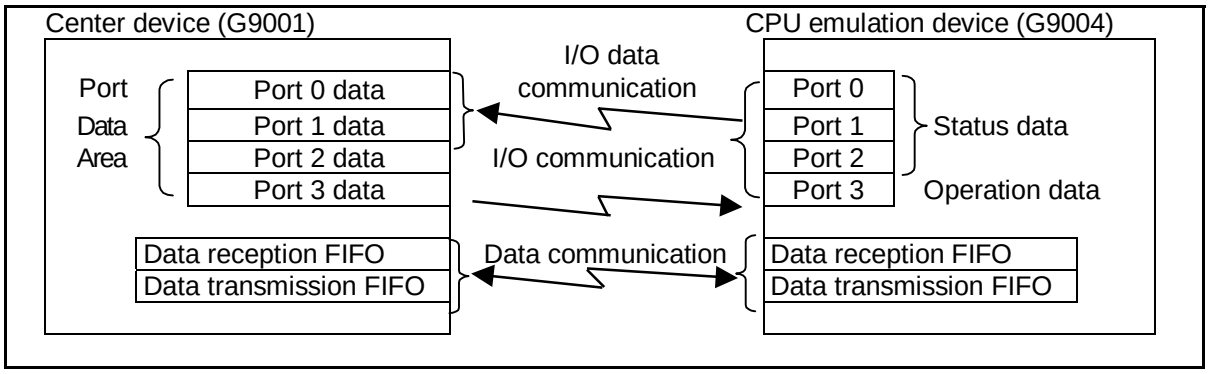
Status 2 (setting information) <Port 2>


7 6 5 4 3 2 1 0
0
Set local operation mode (0: Message communication 1: CPU emulation)
Local CPU interface mode
00: 16-bit interface (2) (68000 etc.)
01: 16-bit I/F (1) (8086,H8 etc.)
10: 8-bit I/F (2) (6809 etc.)
11: 8-bit I/F (1) (Z80 etc.)
Local LCLK setting
Local LWT setting

Operation information <Port 3>

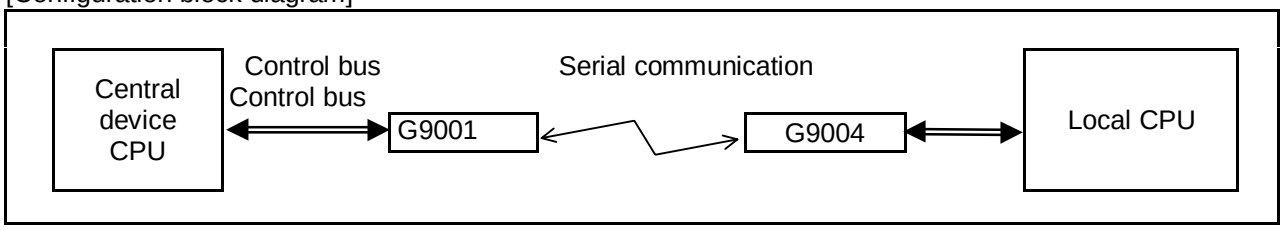


[Communication image]



7. Message communication mode (MOD = LOW)

[Configuration block diagram]



7-1. Terminals for use by a local CPU

Terminal name	I/O	Logic	Description
LIF0	I		Local bus interface mode 0
LIF1	I		Local bus interface mode 1
LRST	O	Negative	Resets the local bus
LA0 to1	I	Positive	Address for local bus lines 0 to 1
LA2 to 5	I	Positive	Pull down to GND (5~10Kohm resistors)
LCS	I	Negative	Chip select for the local bus
LWR	I	Negative	Write signal for the local bus
LRD	I	Negative	Read signal for the local bus
LWRQ	O	Negative	Wait request for the local bus
LIFB	O	Negative	Interface busy for the local bus
LIRQ	O	Negative	Interrupt request for the local bus
LD0 to 7	B	Positive	Low-byte signal for the local bus
LD8 to 15	B	Positive	High-byte signal for the local bus

7-2. I/O map for the local CPU

16-bit interface (1) and (2) (8086, H8, and 68000) [LIF1 = 1]

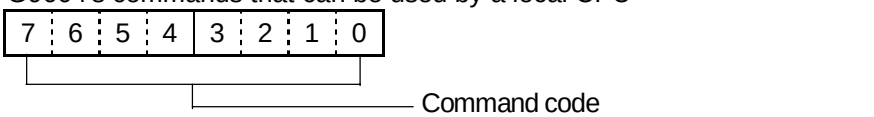
LA1	Writing	Reading
0	Write command	Read status
1	Write transmission data	Read reception data

8-bit I/f (1) and (2) (Z80, 6809 etc.) [LIF1 = H]

LA0 to LA1	Writing	Reading
00	Write command	Read status
01	Invalid	Invalid
10	Write transmission data	Read reception data
11	Invalid	Invalid

7-3. Command and status information that can be used by a local CPU

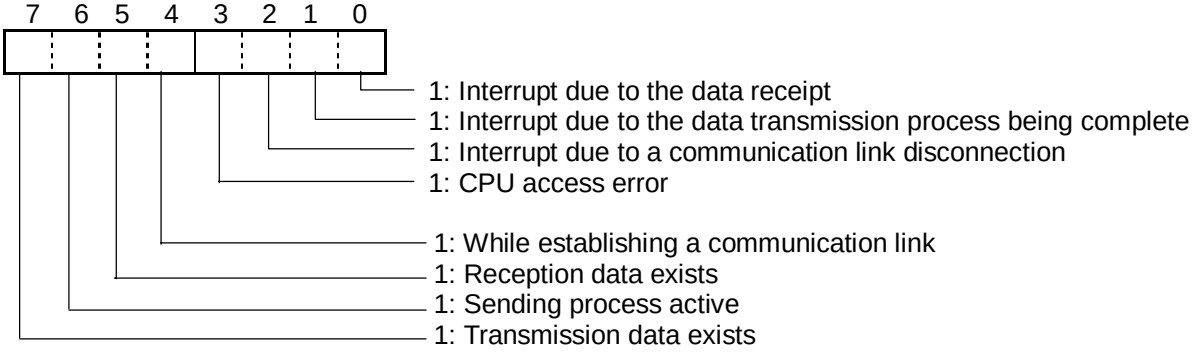
7-3-1. G9004's commands that can be used by a local CPU


7 6 5 4 3 2 1 0
Command code
00h: Invalid
01h: Software reset
02h: Reset transmission FIFO
03h: Reset reception FIFO
04h: Wait for a sending break frame
10h: Data send request

Code	Description
00h	No meaning. (Does not affect the operation)
01h	Software reset. Has the same result as applying a LOW to the RST terminal. See the Note
02h	Resets only the data transmission FIFO. If written during the data sending process (status register bit 6 = 1) it may cause a CPU access error (status register bit 3 = 1).
03h	Resets only the data reception FIFO. Writing this command while no data is being received (status register bit 5 = 0) may cause a CPU access error (status register bit 3 = 1).
04h	The device enters a break frame waiting status. This has the same results as applying a HIGH pulse to the BRK terminal.
10h	Data send request. Make the status register 0 bit 3 in the CPU emulation device equal 1 (set the sending request interrupt), so that the center device will be notified that transmission data exists.

Note: When turning ON the power, a reset signal must be supplied (RST = LOW).

7-3-2. G9004 status information that can be seen from a local CPU


7 6 5 4 3 2 1 0
1: Interrupt due to the data receipt
1: Interrupt due to the data transmission process being complete
1: Interrupt due to a communication link disconnection
1: CPU access error
1: While establishing a communication link
1: Reception data exists
1: Sending process active
1: Transmission data exists

Bit	Item	Description
0	Data receipt interrupt	When the G9004 receives message data from the central device, this bit becomes 1 and an interrupt signal is output (LIRQ = L). After this status register is read, this bit returns to 0. When the device only receives an information command, this bit stays 0 and the device does not output an interrupt.
1	Data transmission process complete interrupt	After writing a data transmission command (10h), when the G9004 receives an information command (reset transmission processing flag: 0002h), this bit becomes 1 and the device outputs an interrupt signal (LIRQ = L). After this status register is read, this bit returns to 0.

Bit	Item	Description
2	Communication link disconnected interrupt	When the interval between sending one data sentence and the next from the central device to the PCL exceeds a specified time (time out), this bit becomes 1, and the device outputs an interrupt signal (LIRQ = L). After reading this status register, the interrupt signal is reset. This is used to monitor the watchdog timer output (1: TOUT = L) After a local CPU writes a command (04h), the TOUT output returns HIGH. Then, if the device does not receive data within the specified interval, this bit becomes 1 again.
3	CPU access error	When the PCL device does any of the following on a command from a CPU, this bit becomes 1, and the device outputs an interrupt signal (LIRQ = L). After this status register is read, this bit returns to 0. - Try to write data to the transmission FIFO during transmission processing (status register bit 6 = 1), or writing a transmission FIFO reset command (02h). - Try to read the reception FIFO even though it has received no data (status register bit 5 = 0), or writing a data reception FIFO reset command (03h).
4	Communication link valid	This bit is used to see if the communication line is connected. When the device detects a change on the communication line, this bit becomes 1. If the communication line does not change within a specified time, this bit becomes 0.
5	Received data exists	When there is message data in the data reception FIFO, this bit becomes 1.
6	Data transmission in progress	After writing the data transmission command (10h), this bit becomes 1. When data communication with the center device is complete (when a receiving information command 0002h issued by the central device), this bit becomes 0.
7	Transmission data exists	If there is message data in the data transmission FIFO, this bit becomes 1.

7-4. Information command for the center device (G9001)

To send a message, the first word in the transmission FIFO of the center device is used for the information command.
The remaining 127 words can be used freely as message data (any format is allowed).

Center device transmission FIFO		
Address	Upper	Lower
00h	Information command	
01h to 7Fh	Message data (any format)	

[Information command]

Command code	Description
0001h	Message transmission. Use this command to send a message or data from the center device to a local CPU. You can attach a message or data at the end of this command. (There is also an Information command without any message.)
0002h	When the G9004 receives this command, the data transmission process complete interrupt < local status register bit 1 = 1 > and the device resets the transmission processing flag < local status register bit 6 >. You can attach a message or data at the end of this command.
0003h	Resend request command When the G9004 receives this command, it sends the same data as it last sent. Use this command when the center device cannot receive data from the local device due a data communication error or other reason.

7-5. Message communication procedure

The device model numbers are shown in parenthesis.
Numbers marked with ( ) mean that the operations are carried out by a CPU.
Assume that the local device address (for the G9004) is "08h."
In addition, the port status information for the I/O cycle communication or data communication is sent to the port data area in the center device (G9001). In order to generate an interrupt (position *1) in the center device (G9001) when an interrupt request (bit 0 = 1 on port 0) occurs in the local device (G9004), you must enable the input change interrupt that corresponds to port 0 (set it to 1).

(1) When the center device (G9001) is the first to send a message and the local device (G9004) responds

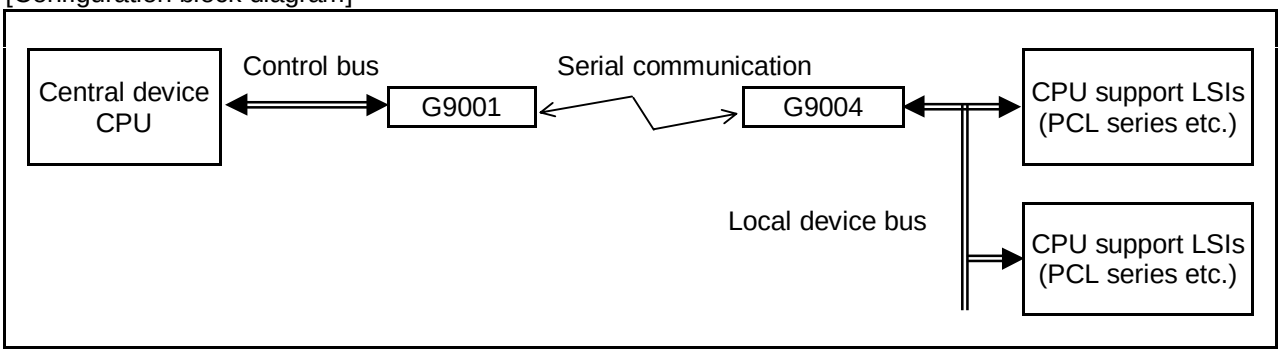
[Center device (G9001)]	[Local device (G9004)]
[Start]	
(1) Write an information command (0001h: Message transmission) to the data transmission FIFO. (2) Place a message in the data transmission FIFO. (3) Write a data communication command (4008h).	
********** Data communication (1st time) **********	
- Interrupt occurs (4) The center device reads the status. ▽ Data transmission complete <bit 0=1>	- Interrupt occurs (1) Read the status ▽ Data reception interrupt <bit 0 = 1> (2) Read the message in the data reception FIFO. (3) Place the message in the data transmission FIFO. (4) Write a data transmission command (10h). - Set the status for port 0 (interrupt information) ▼ Local device data transmission request interrupt <Bit 1 = 1>
*1 - Interrupt occurs <- - - -

(2) When the local device (G9004) is the first to send a message and the center device (G9001) responds

[Center device (G9001)]	[Local device (G9004)]
[Start]	
*1 - Interrupt occurs ← (1) Read the central device status ▽ Input change interrupt <bit 3=1> (2) Reset the input change interrupt (3) Send an information command (0001h: message transmission) to the data transmission FIFO. (4) Place a message in the data transmission FIFO. (5) Write a data communication command (4008h).	(1) Place a message in the data transmission FIFO. (2) Write a data send command (10h). - Set the status for port 0 (interrupt information) ▼ Local device data send request interrupt <bit 1 = 1> ▼ Local device interrupt request <bit 0 = 1>
********** Data communication (1st time) **********	
	After receiving a message from the central device, the local device sends the data in the FIFO to the central device.
- Interrupt occurs (6) The central device reads the status. ▽ Data communication compete <bit 0 = 1> (7) Read the message in the data reception FIFO. (8) Send an information command (0002h: Reset the data send processing flag) to the data transmission FIFO. This is how the center device informs the local device that the data was received normally. (9) Write a data communication command (4008h).	- Interrupt occurs (3) The local device reads the status. ▽ Data received interrupt <Bit 0=1> (4) Read the message in the data reception FIFO.
********** Data communication (2nd time) **********	
- Interrupt occurs (10) Read the status ▽ Data communication compete <bit 0 = 1>	- Reset data transmission FIFO. - Interrupt occurs (5) Read the status of the local device ▽ Data transmission process complete interrupt <bit 1=1>
[End of message communication]	

8. CPU emulation mode (MOD = H)

[Configuration block diagram]



8-1. Terminals on the G9004

Terminal name	I/O	Logic	Description
LIF0	I		Local bus interface mode 0
LIF1	I		Local bus interface mode 1
LWT0	I	Positive	Local bus interval time setting 0
LWT1	I	Positive	Local bus interval time setting 1
LRST	O	Negative	Local bus reset
LA0 to LA5	O	Positive	Local bus address
LCS	O	Negative	Local bus chip select
LWR	O	Negative	Local bus write signal
LRD	O	Negative	Local bus read signal
LWRQ	I	Negative	Local bus wait request
LIRQ	I	Negative	Local bus interrupt request
LD0 to LD7	B	Positive	Local bus data 0 to 7
LD8 to LD15	B	Positive	Local bus data 8 to 15

Shown below are representative CPUs and the corresponding terminals on the G9004.

Typical CPU		G9004	
CPU name	Terminal name	G9004 terminal name	G9004 mode
Z80	$\overline{RD}$	LRD	8 bit interface (1)
	$\overline{WR}$	LWR	
8086	$\overline{RD}$	LRD	16 bit interface (1)
	$\overline{WR}$	LWR	
	Upper enable	None	
	Lower enable	None	
68000	R/$\overline{W}$	LWR	16 bit interface (2)
	Upper strobe	LRD (No distinction between upper/lower)	
	Lower strobe	LRD (No distinction between upper/lower)	
H8	$\overline{RD}$	LRD	16 bit interface (1)
	Upper WR	LWR (No distinction between upper/lower)	
	Lower WR	LWR (No distinction between upper/lower)	
6809	R/$\overline{W}$	LWR	8 bit interface (2)
	E	LRD	

8-2. Control method for using a central device (G9001)

When you want to perform CPU emulation using the G9004, write the commands and data using the formats specified for the data transmission FIFO in the central device (G9001). The center device's data transmission FIFO can store up to 128 words, including write commands, write data, and read commands.

When writing data, there is no data to be sent from the G9004. But, when reading data, the G9004 will send a read command and then read data from the center device

Therefore, more than 128 words of data cannot be handled by the G9004.

[When writing data]

Central device data transmission FIFO		
Address	Upper	Lower
00h	Command (writing)	
01h	Writing data (1)	
02h	Writing data (2)	
-	-	
-	-	
-	-	

[When reading data]

Central device data transmission FIFO		
Address	Upper	Lower
00h	Command (reading)	
01h	Command (reading)	
02h	Command (reading)	
-	-	
-	-	
-	-	

[Combined case]

Central device data transmission FIFO		
Address	Upper	Lower
00h	Command (writing)	
01h	Writing data (1)	
02h	Writing data (2)	
03h	Command (reading)	
04h	Command (writing)	
05h	Writing data	
-	-	
-	-	

If the G9004 is set up to use an 8-bit CPU interface, the following precautions should be noted.

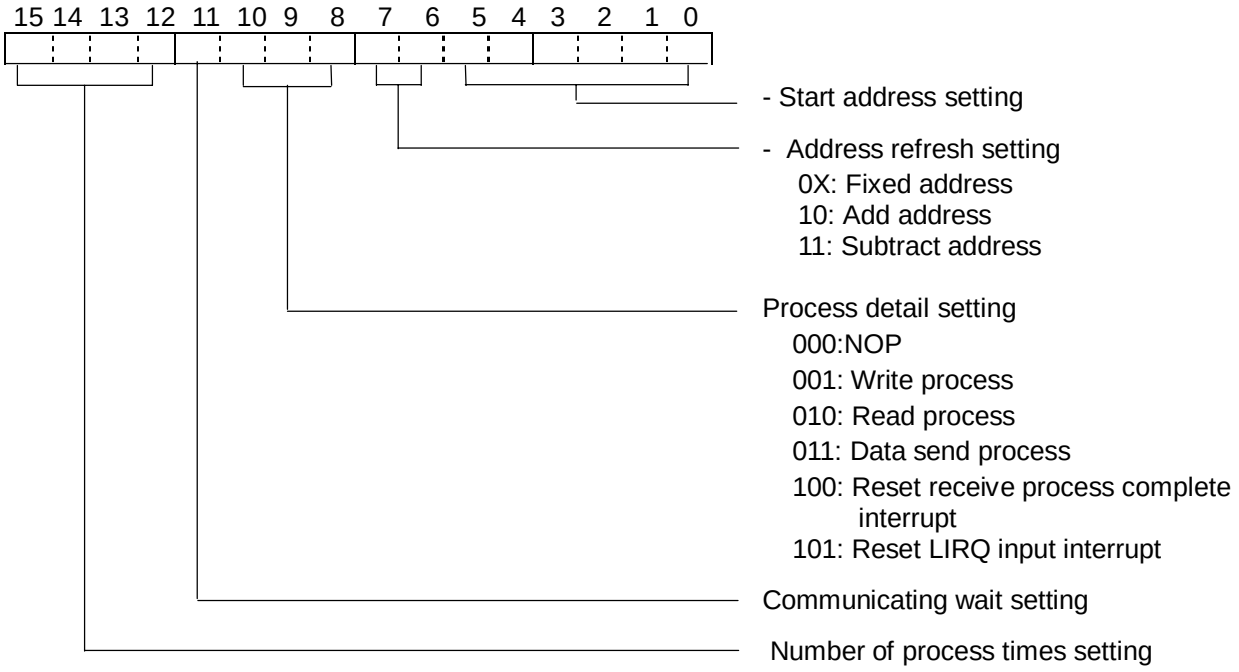
- When the central device (G9001) uses a 16-bit interface
  An even number of data bytes must always be written. However, if the number of bytes that the G9004 requests is odd, the last byte will be thrown away (the final write operation will not be executed). Instead, the G9001 will execute the next operation command.
  When the number of bytes to read is odd, the last byte of the data sent from the G9004 must be dummy data.

- When the center device (G9001) uses an 8-bit interface
  The operation command for the G9004 must be written to the same address in the central device (G9001) data transmission FIFO by arranging the upper and lower bytes in order. If the number of data bytes to write is odd, write one dummy data byte to make the total even. Then use the following operation commands for the G9004 at the same address.
  Shown below is an example where 3 bytes of data are to be written. Write a dummy data byte to the upper 8 bits of address 02h.

Central device (G9001) data transmission FIFO data		
Address	Upper 8 bytes	Lower 8 bytes
00h	Write command (upper)	Write command (lower)
01h	Write data 2	Write data 1
02h	Write data 4 (dummy data)	Write data 3
03h	Write command (upper)	Write command (lower) ◀
04h	Write data 5	Write data 4
05h	-	-
06h	-	-

Write the operation commands to the same addresses.

8-2-1. Command


15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
- Start address setting
- Address refresh setting
0X: Fixed address
10: Add address
11: Subtract address
Process detail setting
000:NOP
001: Write process
010: Read process
011: Data send process
100: Reset receive process complete interrupt
101: Reset LIRQ input interrupt
Communicating wait setting
Number of process times setting

◆ Start address setting
- Set the top address for the read or write process.
- If the CPU emulation device (G9004) is using a 16-bit CPU interface, the lower bit setting is ignored and always treated as 0.
- Commands other than writing and reading processes are invalid.

◆ Address refresh setting
- When the number of processing times does not equal zero, select an address refresh method
- When the number of processing times is 0, commands other than writing and reading processes are invalid.

◆ Process detail setting
- Select the processing detail for the CPU emulation device (G9004)

Item	Processing detail
NOP	"Do-nothing" command. The device does nothing.
Read process	The CPU emulation device (G9004) reads the number of bytes specified in the processing register, starting from the start address.
Write process	The CPU emulation device (G9004) writes the number of bytes specified in the processing register, starting from the start address.
Data send process	The device sends the data that was read by using the read process to the central device. In addition, if the reception process complete interrupt flag (bit 1 on port 0) is 1, and this command is received, the device will send the same data as it last sent (the data resend process).
Reset the reception process complete interrupt flag	Reset the reception process complete interrupt flag (bit 1 on port 0) to 0.
LIRQ input interrupt reset	Reset the LIRQ input interrupt (bit 2 on port 0) to 0.

◆ Communication wait setting

- Select whether to use the communication wait time during the reading and writing processes.
- When set to 0, the G9004 will return the normal response (without data) soon after receiving a command from the central device (G9001).
- When set to 1, the G9004 will wait a maximum of 10 μsec (at 20 Mbps) to respond after receiving a command from the central device (G9001). While waiting, if the received processes are all complete and there is a read command, the device will send read data. If there is no read command, or if the received processes do not complete within the waiting time, it sends a normal response (without data).
- Commands other than writing/reading processes are invalid.
- The only valid setting is for the 1st word (01h address) in the central device data transmission FIFO. Setting it to any other address is not allowed.

◆ Processing bytes setting

- Set the number of processing bytes when you want to read or write continuously. (Set a burst cycle). Enter (the number of processing bytes - 1) as the setting.
  When the device is used with a 16-bit CPU interface, set the number in units of words.
  Otherwise, when the device is used with an 8-bit CPU interface, set the number in units of bytes.
  Commands other than write/read processes are not allowed.

8-2-2. Examples of CPU emulation control procedures

The device model number is shown in parenthesis.
Numbers marked with ( ) mean that the operations are carried out by a central device (G9001) emulating a CPU.
Assume that the local device address (for the G9004) is "08h."
In addition, the port status information of the I/O cycle communication or data communication is sent to the port data area of the central device (G9001). In order to generate an interrupt (position *1) in the central device (G9001) when an interrupt request (bit 0 = 1 on port 0) occurs in the local device (G9004), you must enable the input change interrupt that corresponds to port 0 (set it to 1).

8-2-2-1. Examples of writing single units of data (16-bit CPU interface)

[Write the data 1234h to address 2] (without using communication wait time)

[Center device (G9001)]	[Local device (G9004)]
[Start]	
(1) Place a command (0102h) in the data transmission FIFO. (2) Place the data (1234h) into the data transmission FIFO. (3) Write a data communication command (4008h).	
********** Data communication (1st time) **********	
- Interrupt occurs (4) The central device reads the status ▽ Data communication complete <bit 0=1>	1. Write 1234h to address 2. 2. Set status port 0 (interrupt information) ▼ Receive process complete interrupt <bit 1=1>
*1	
- Interrupt occurs ←	▼ Interrupt request <Bit 0=1>
(5) The central device reads the status ▽ Input change interrupt<Bit 3=1> (6) Write (0400h) to the data transmission FIFO. [Reset reception process complete interrupt]. (7) Write a data communication command (4008h)	
********** Data communication (2nd time) **********	
- Interrupt occurs (8) The central device reads the status. ▽ Data communication complete <Bit 0=1>	
[End emulation communication]	

Data transmission FIFO

Address	Upper	Lower
00h	01h	02h
01h	12h	34h

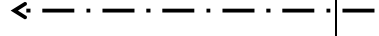
Data transmission FIFO

Address	Upper	Lower
00h	04h	00h

8-2-2-2. Example of writing continuous data (16-bit CPU interface)

[Write 1234h to address 4, 2345h to address 6, and 3456h to address 8] (Without a communication wait time)

<table>
<tr><th>[Center device (G9001)]</th><th>[Local device (G9004)]</th></tr>
<tr><td colspan="2">[Start]</td></tr>
<tr><td>(1) Place a command (2184h) in the data transmission
<table>
<tr><th colspan="3">Data transmission FIFO</th></tr>
<tr><th>Address</th><th>Upper</th><th>Lower</th></tr>
<tr><td>00h</td><td>21h</td><td>84h</td></tr>
<tr><td>01h</td><td>12h</td><td>34h</td></tr>
<tr><td>02h</td><td>23h</td><td>45h</td></tr>
<tr><td>03h</td><td>34h</td><td>56h</td></tr>
</table>
(2) Place data (1234h) in the data transmission FIFO.
(3) Place data (2345h) in the data transmission FIFO.
(4) Place data (3456h) in the data transmission FIFO.
(5) Write a data communication command (4008h).</td><td></td></tr>
<tr><td colspan="2">********** Data communication (1st time) **********</td></tr>
<tr><td>- Interrupt occurs
(6) The central device reads the status.
▽ Data communication complete <bit 0=1>

*1
Interrupt occurs 

(7) The central device reads the status.
▽ Input change interrupt <bit 3=1>
(8) Reset the input change interrupt
(9) Place a command (0400h) in the data transmission FIFO.
<table>
<tr><th colspan="3">Data transmission FIFO</th></tr>
<tr><th>Address</th><th>Upper</th><th>Lower</th></tr>
<tr><td>00h</td><td>04h</td><td>00h</td></tr>
</table>
[Reset reception process complete interrupt]
(10) Write a data communication command (4008h).</td><td>1. Write 1234h to address 4.
2. Write 2345h to address 6.
3. Write 3456h to address 8.
4. Set the status on port 0 (interrupt information).
▼ Receive process complete interrupt <Bit 1 = 1>
▼ Interrupt request <Bit 0=1></td></tr>
<tr><td colspan="2">********** Data communication (2nd time) **********</td></tr>
<tr><td>- Interrupt occurs
(11) Central device reads the status.
▽ Data communication complete <Bit 0=1></td><td></td></tr>
<tr><td colspan="2">[End emulation communication]</td></tr>
</table>

8-2-2-3. Example of reading continuous data (16-bit CPU interface)

[Read data addresses 16, 14, 12, and 10 in this order] (Using a communication wait time)

<table>
<tr><th>[Center device (G9001)]</th><th>[Local device (G9004)]</th></tr>
<tr><td colspan="2">[Start]</td></tr>
<tr><td>(1) Place a command (3AD0h) in the data transmission FIFO.
<table><tr><th colspan="3">Data transmission FIFO</th></tr><tr><th>Address</th><th>Upper</th><th>Lower</th></tr><tr><td>00h</td><td>3Ah</td><td>D0h</td></tr></table>
(2) Write a data communication command (4008h).</td><td></td></tr>
<tr><td colspan="2">********** Data communication (1st time) **********</td></tr>
<tr><td>Wait time</td><td>1. Place a command (3AD0h) in the data transmission FIFO.
<table><tr><th colspan="3">Data transmission FIFO</th></tr><tr><th>Address</th><th>Upper</th><th>Lower</th></tr><tr><td>00h</td><td>3Ah</td><td>D0h</td></tr><tr><td>01h</td><td>FFh</td><td>EEh</td></tr><tr><td>02h</td><td>DDh</td><td>CCh</td></tr><tr><td>03h</td><td>BBh</td><td>AAh</td></tr><tr><td>04h</td><td>99h</td><td>88h</td></tr></table>
2. Read from address 16 (FFEEh) and write to the data transmission FIFO.
3. Read from address 14 (DDCCh) and write to the data transmission FIFO.
4. Read from address 12 (BBAAh) and write to the data transmission FIFO.
5. Read from address 10 (9988h) and write to the data transmission FIFO.
6. Set the status for port 0 (interrupt information)
▼ Receive process complete interrupt <Bit 1=1>
▼ Interrupt request <Bit 0=1>
7. Send the FIFO contents to the central device.</td></tr>
<tr><td>- Interrupt occurs
(3) The central device reads the status
▽ Data communication complete <bit 0=1>
▽ Input change interrupt <bit 3=1>
(4) Reset the input change interrupt
(5) Read from the reception FIFO
(6) Place a command (0400h) in the data transmission FIFO.
<table><tr><th colspan="3">Data transmission FIFO</th></tr><tr><th>Address</th><th>Upper</th><th>Lower</th></tr><tr><td>00h</td><td>04h</td><td>00h</td></tr></table>
[Reset the reception process complete interrupt]
(7) Write a data communication command (4008h).</td><td></td></tr>
<tr><td colspan="2">********** Data communication (2nd time) **********</td></tr>
<tr><td>- Interrupt occurs
(8) Read the central device status
▽ Data communication complete <bit 0=1></td><td></td></tr>
<tr><td colspan="2">[End emulation communication]</td></tr>
</table>

[Read, in order, from address 16, 14, 12, and 10] (Without a communication wait time)

Center device (G9001)]	[Local device (G9004)]
[Start]	
(1) Place a command (32D0h) in the data transmission FIFO. (2) Write a data communication command (4008h). Data transmission FIFO: Address 00h, Upper 32h, Lower D0h	
********** Data communication (1st time) **********	
- Interrupt occurs (3) Read the status ▽ Data communication complete <Bit 0=1>	1. Place a command (32D0h) in the data transmission FIFO. 2. Read address 16 (FFEEh) and write it to the data transmission FIFO. 3. Read address14 (DDCCh) and write it to the data transmission FIFO. 4. Read address12 (BBAAh) and write it to the data transmission FIFO. 5. Read address10 (9988h) and write it to the data transmission FIFO. 6. Set port 0 (interrupt information) ▼ Receive process complete interrupt <Bit 1=1> ▼ Interrupt request <Bit 0=1> Data transmission FIFO: Address 00h, Upper 3Ah, Lower D0h Address 01h, Upper FFh, Lower EEh Address 02h, Upper DDh, Lower CCh Address 03h, Upper BBh, Lower AAh Address 04h, Upper 99h, Lower 88h
*1 - Interrupt occurs (4) The central device reads the status ▽ Input change interrupt <bit 3=1> (5) Reset the input change interrupt. (6) Place a command (0300h) in the data transmission FIFO. [Data sending process] (7) Write a data communication command (4008h). Data transmission FIFO: Address 00h, Upper 03h, Lower D0h	
	Send the contents of the data transmission FIFO to the central device.
********** Data communication (2nd time) **********	
- Interrupt occurs (8) The central device reads the status. ▽ Data communication complete <bit 0=1> (9) Read data from the data reception FIFO. (10) Place a command (0400h) in the data transmission FIFO. [Reset the rseceive process complete interrupt] (11) Write a data communication command (4008h). Data transmission FIFO: Address 00h, Upper 04h, Lower 00h	
********** Data communication (3rd time) **********	
- Interrupt occurs (12) The central device reads the status. ▽ Data communication complete <bit 0=1>	
[End emulation communication]	

8-2-2-4. Example of combined processing (16-bit CPU interface)

[After writing 1234h to address 0, read addresses 4 and 6] (With a communication wait time)

[Center device (G9001)]	[Local device (G9004)]
[Start]	
(1) Place a command (0100h) in the data transmission FIFO. (2) Place data (1234h) in the data transmission FIFO. (3) Place a command (1284h) in the data transmission FIFO. (4) Write a data communication command (4008h).	
********** Data communication (1st time) **********	
Wait time	1. Write 1234h to address 0. 2. Place a command (1284h) in the data transmission FIFO. 3.Read from address 4 (FFEEh) and write it to the data transmission FIFO. 4.Read from address 6 (DDCCh) and write it to the data transmission FIFO. 5. Set the status for port 0 (interrupt information) ▼ Receive process complete interrupt <Bit 1=1> ▼ Write request <Bit 0=1> 6. Send the contents of the data transmission FIFO to the central device.
- Interrupt occurs (5) The central device reads the status. ▽ Data communication complete <Bit 0=1> ▽ Input change interrupt <Bit 3=1> (6) Reset the input change interrupt (7) Read the data from the data reception FIFO. (8) Write b(0400h) to the data transmission FIFO. [Reset the receive process complete interrupt] (9) Write a data communication command (4008h).	
********** Data communication (2nd time) **********	
- Interrupt occurs. (10) The central device reads the status. ▽ Data communication complete <Bit 0=1>	
[End of emulation communication]	

Data transmission FIFO

Address	Upper	Lower
00h	01h	00h
01h	12h	34h
02h	12h	84h

Data transmission FIFO

Address	Upper	Lower
00h	12h	84h
01h	EEh	FFh
02h	DDh	CCh

Data transmission FIFO

Address	Upper	Lower
00h	04h	00h

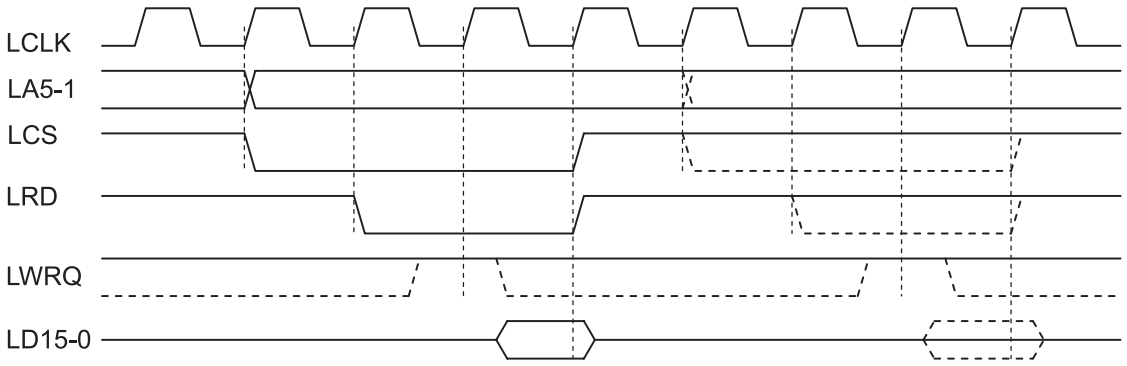
[After writing 1234h to address 0, read addresses 4 and 6] (Without a communication wait time)

[Center device (9001)]	[Local device (9004)]
[Start]	
(1) Place a command (0100h) in the data transmission FIFO. (2) Place data (1234h) in the data transmission FIFO. (3) Place a command (1284h) in the data transmission FIFO. (4) Write a data communication command (4008h). Data transmission FIFO: Address 00h: Upper 01h, Lower 00h; Address 01h: Upper 12h, Lower 34h; Address 02h: Upper 12h, Lower 84h	
********** Data communication (1st time) **********	
- Interrupt occurs (5) The central device reads the status. ▽ Data communication complete <Bit 0=1>	1. Write 1234h to address 0. 2. Place a command (1284h) in the data transmission FIFO. 3. Read from address 4 (FFEEh) and write it to the data transmission FIFO. 4. Read from address 6 (DDCCh) and write it to the data transmission FIFO. 5. Set the status on port 0 (interrupt information). ▼ Receive process complete interrupt <Bit 1 = 1> ▼ Interrupt request <Bit 0=1> Data transmission FIFO: Address 00h: Upper 12h, Lower 84h; Address 01h: Upper FFh, Lower EEh; Address 02h: Upper DDh, Lower CCh
*1 - Interrupt occurs ← (6) The central device reads the status. ▽ Input change interrupt <Bit 3=1> (7) Reset the input change interrupt. Write (0300h) to the data transmission FIFO. [Data sending process] (8) Write a data communication command (4008h) Data transmission FIFO: Address 00h: Upper 03h, Lower 00h	
	Send the contents of the data transmission FIFO to the central device.
********** Data communication (2nd time) **********	
- Interrupt occurs (10) The central device reads the status. ▽ Complete data communication <bit 0=1> (11) Read the data from the data receipt FIFO. (12) Place a command (0400h) in the data transmission FIFO. [Reset the reception process complete interrupt] (13) Write a data communication command (4008h). Data transmission FIFO: Address 00h: Upper 04h, Lower 00h	
********** Data communication (3rd time) **********	
- Interrupt occurs (14) The central device reads the status. ▽ Compete data communication <Bit 0=1>	
[End emulation communication]	

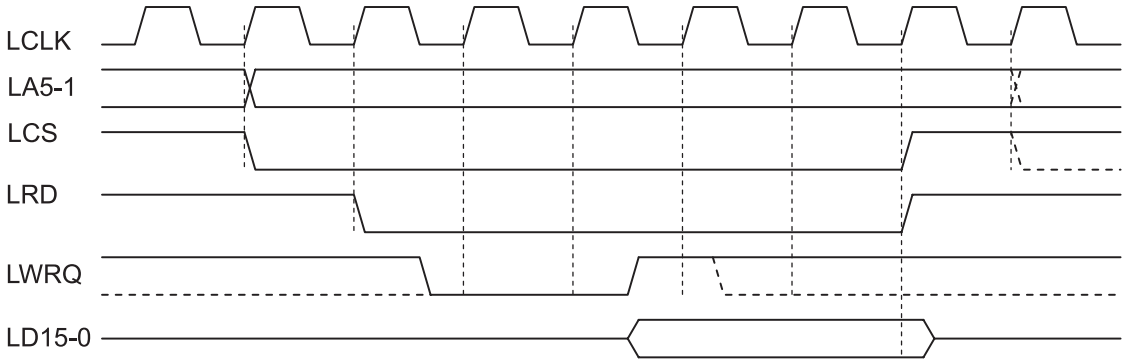
8-3. Emulation timing

8-3-1.16-bit CPU I/F (1) (8086, H8 etc.)

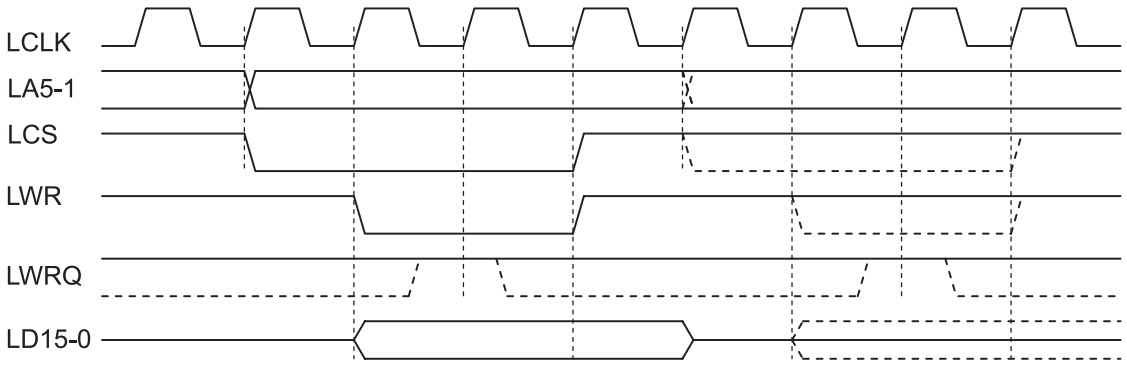
8-3-1-1. Read cycle (1) (without a wait cycle)



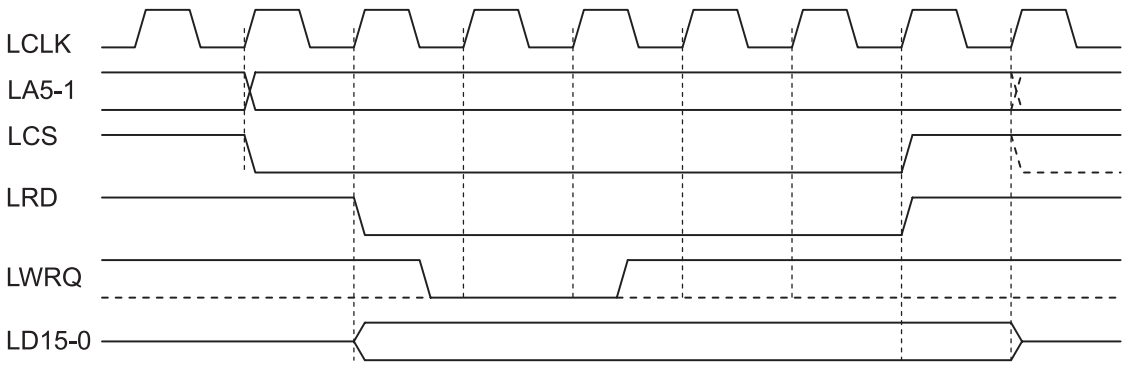
8-3-1-2. Read cycle (2) (wait 2 cycles)



8-3-1-3. Write cycle (1) (without a wait cycle)

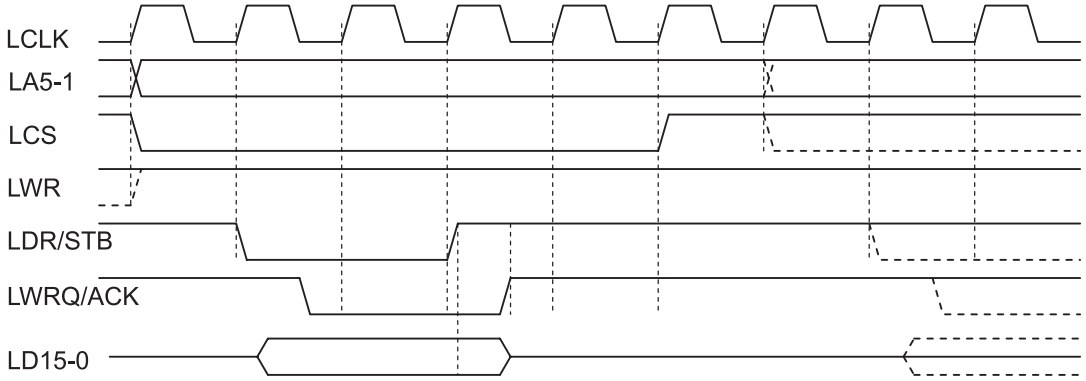


8-3-1-4. Write cycle (2) (wait 2 cycles)

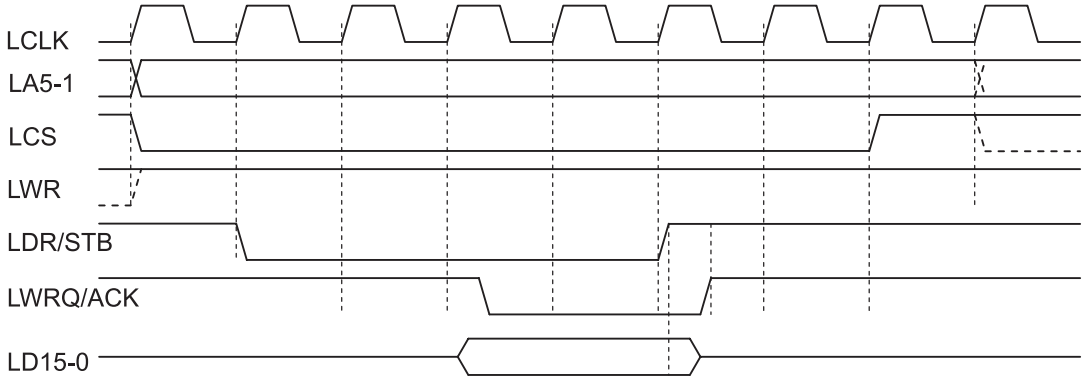


8-3-2.16-bit CPU I/F (2) (68000 etc.)

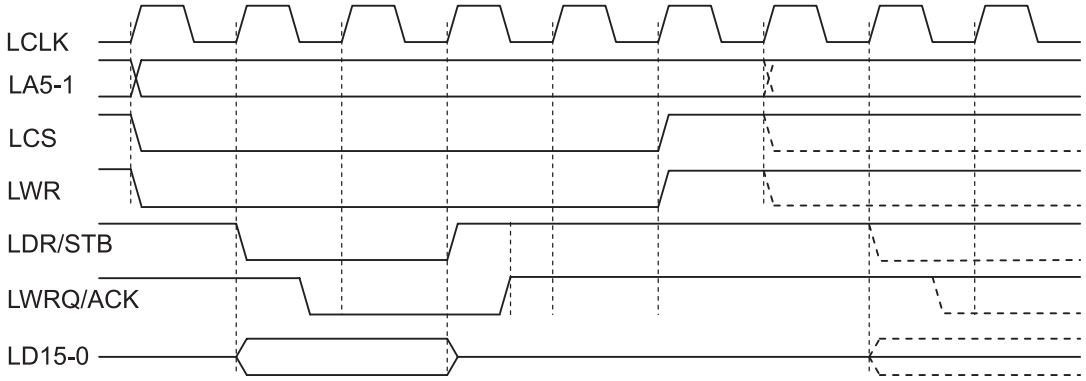
8-3-2-1. Read cycle (1) (without a wait cycle)



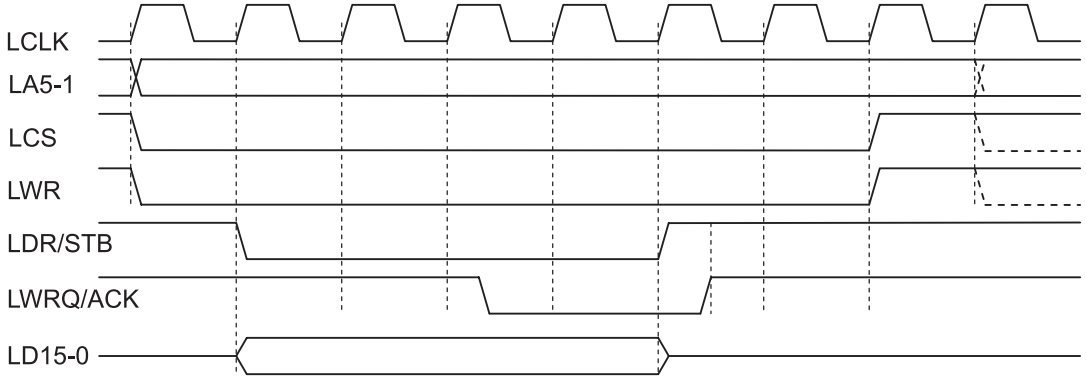
8-3-2-2. Read cycle (2) (wait 2 cycles)



8-3-2-3. Write cycle (1) (without a wait cycle)

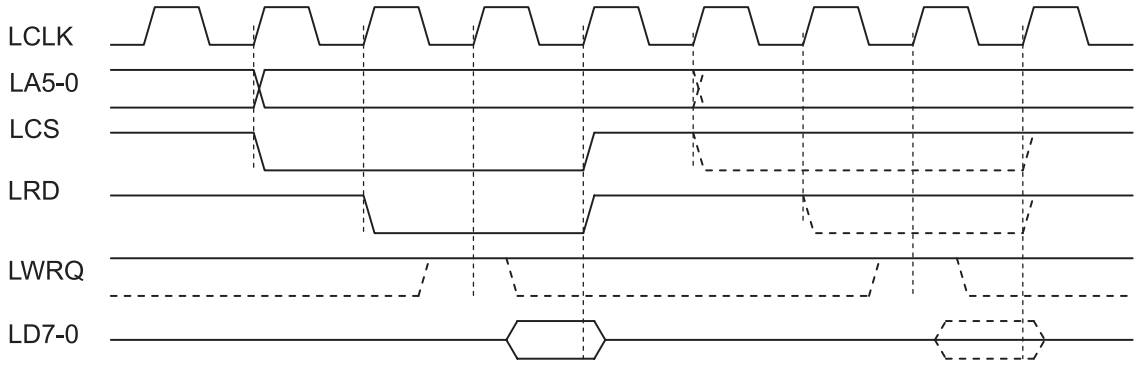


8-3-2-4. Write cycle (2) (wait 2 cycles)

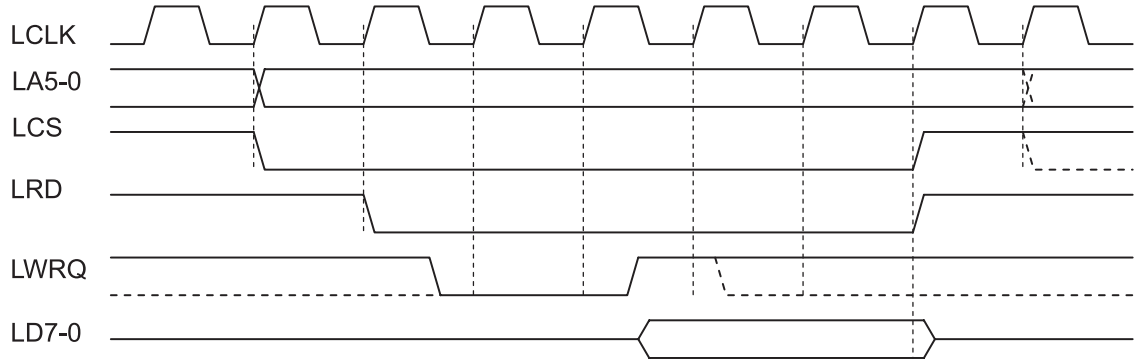


8-3-3. 8-bit CPU I/F (1) (Z80 etc.)

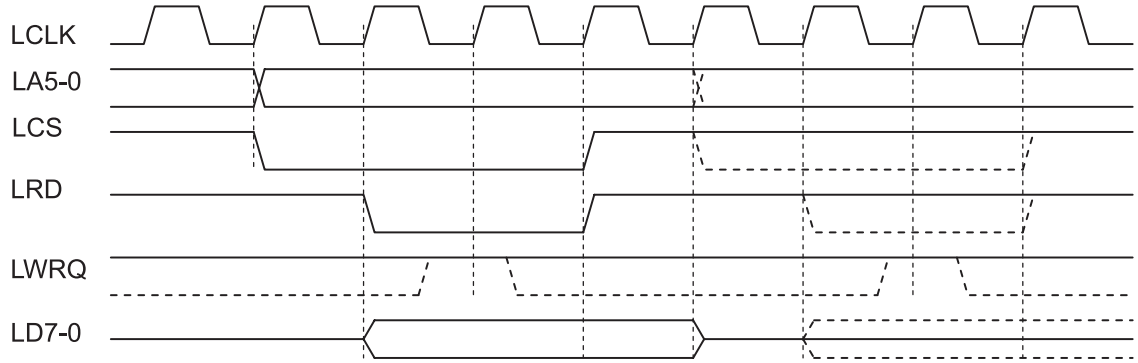
8-3-3-1. Read cycle (1) (without a wait cycle)



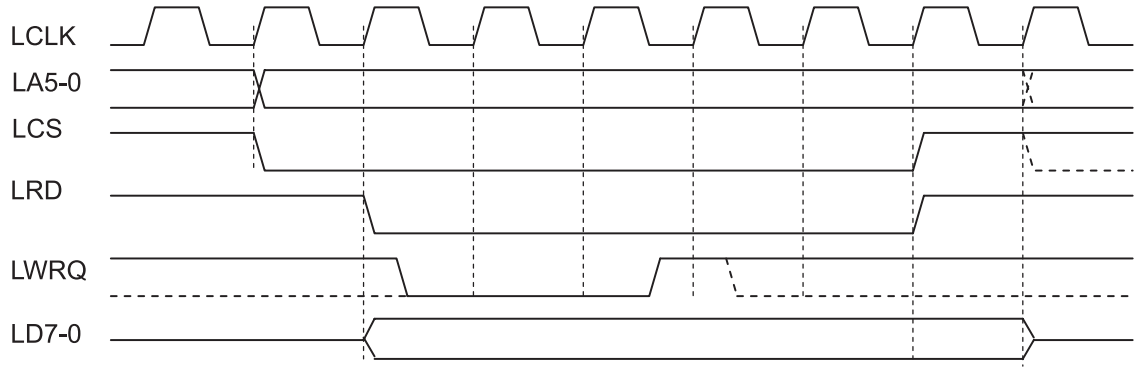
8-3-3-2. Read cycle (2) (wait 2 cycles)



8-3-3-3. Write cycle (1) (without a wait cycle)

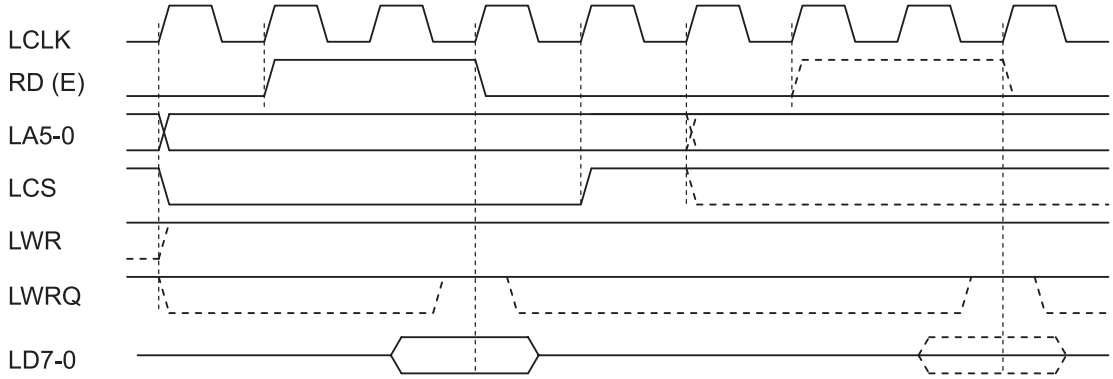


8-3-3-4. Write cycle (2) (wait 2 cycles)

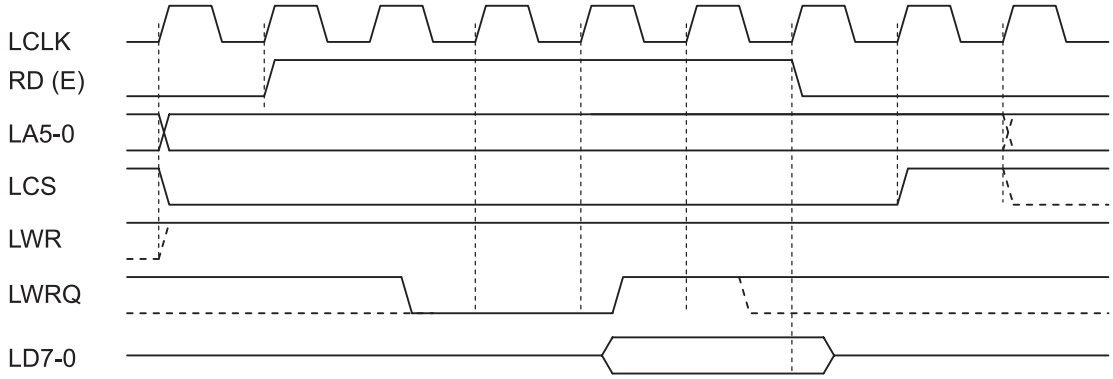


8-3-4. 8-bit CPU I/F (2) (6809 etc.)

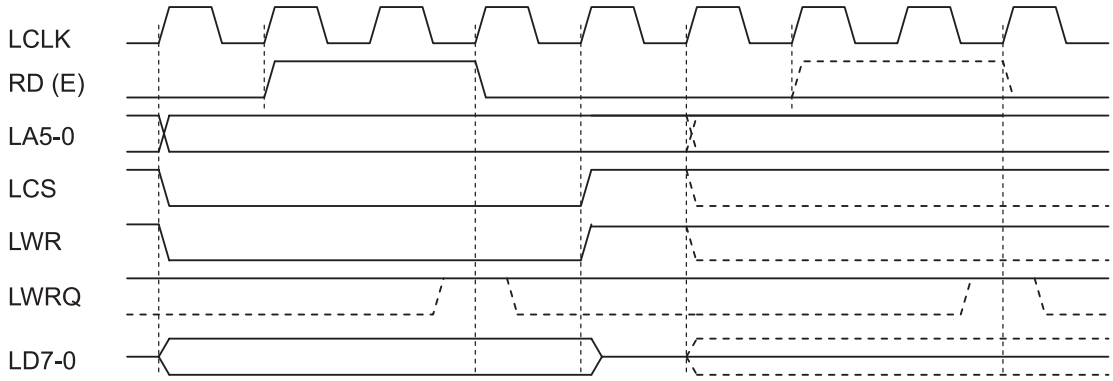
8-3-4-1. Read cycle (1) (without a wait cycle)



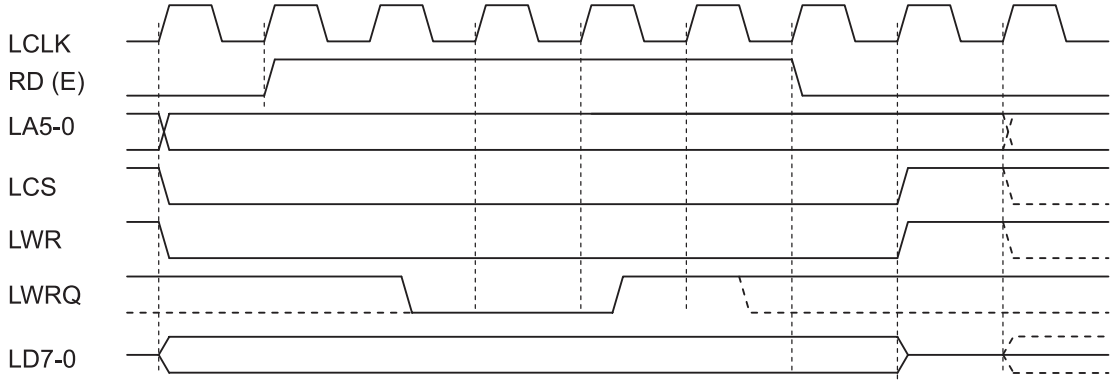
8-3-4-2. Read cycle (2) (wait 2 cycles)



8-3-4-3. Write cycle (1) (without a wait cycle)

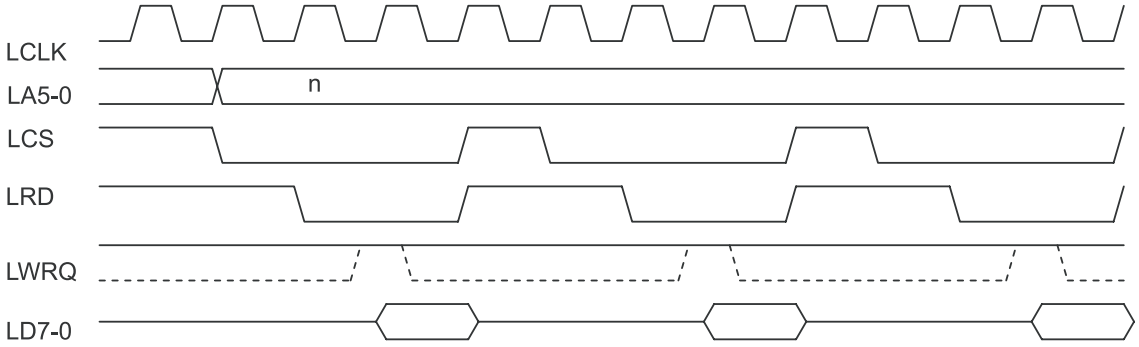


8-3-4-4. Write cycle (2) (wait 2 cycles)

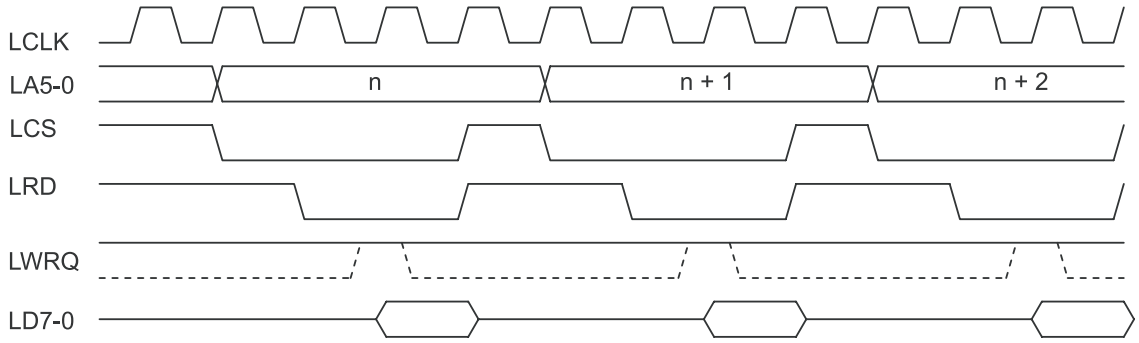


8-4-5. Example of a burst cycle (8-bit CPU-I/F (1) (Z80 etc.)

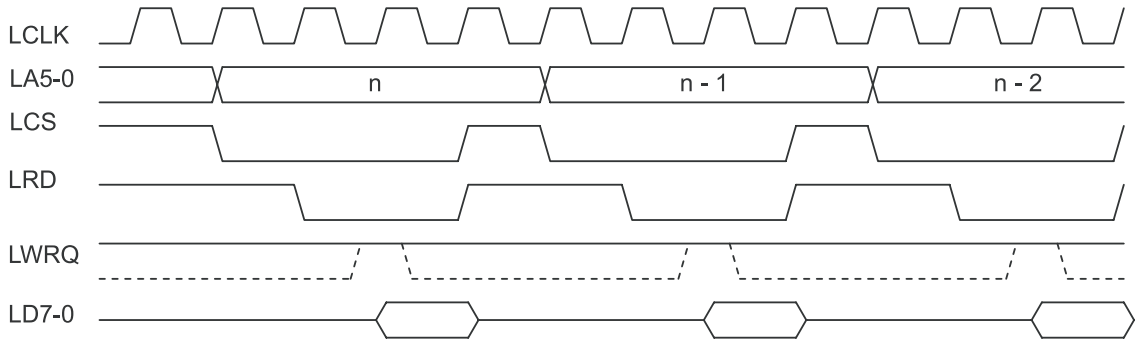
8-4-5-1. Burst read cycle (1) (Fixed address)



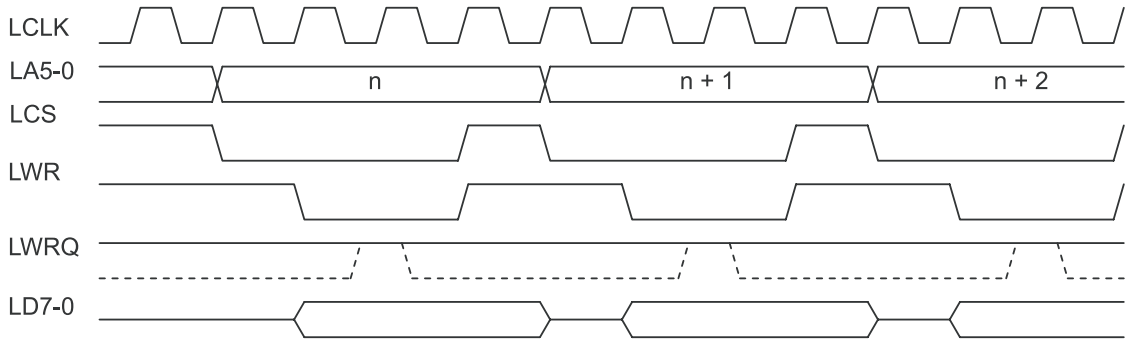
8-4-5-2. Burst read cycle (2) (add an address)



8-4-5-3. Burst read cycle (3) (subtract an address)



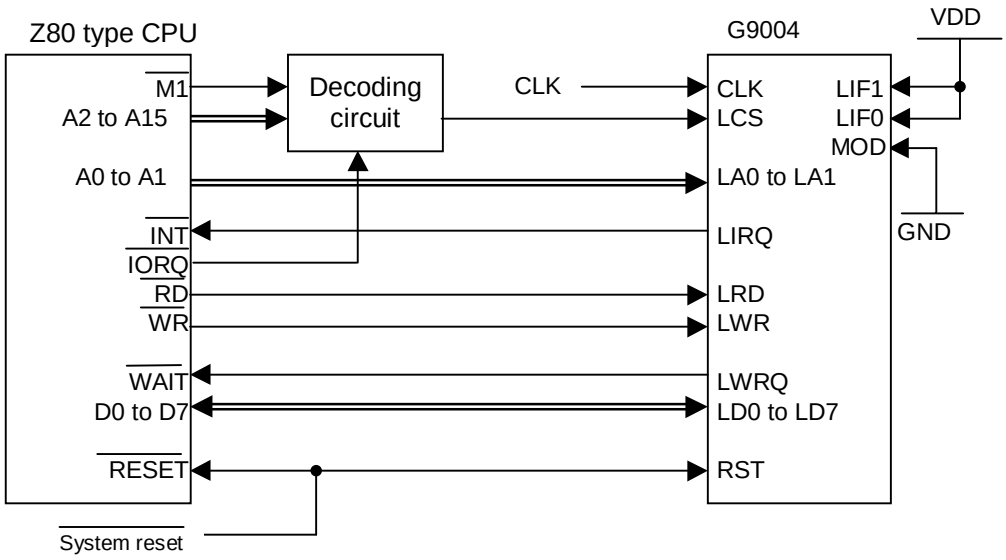
8-4-5-4. Burst write cycle (add an address)



9. Connection examples and recommended environment

9-1. Example of a connection to a CPU using the CPU message communication mode (MOD = L).

9-1-1. 8-bit I/F (1) (IF1 = HIGH, IF0 = HIGH)

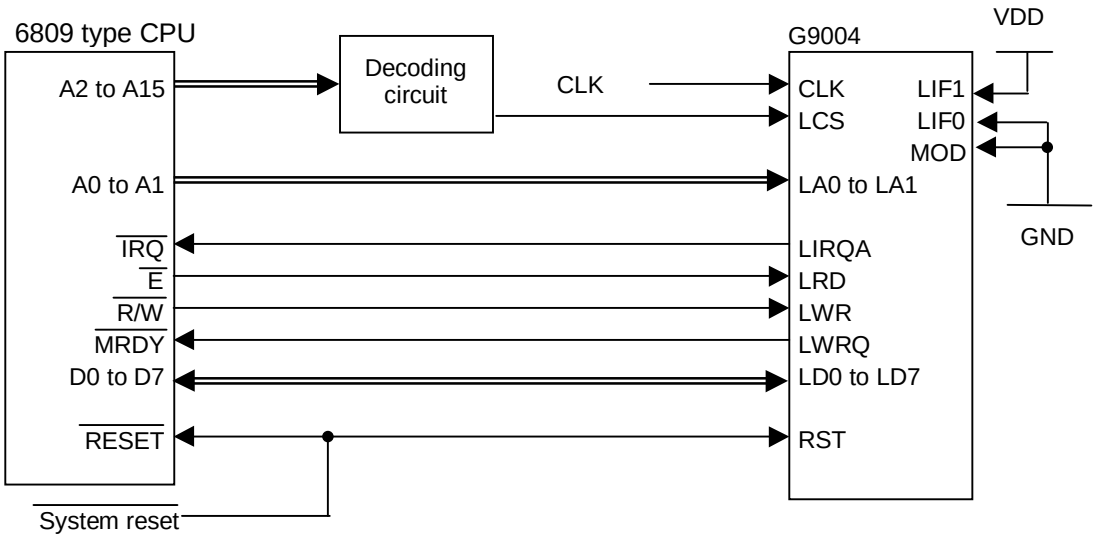


Note 1: When you use an interrupt controller, the CPU will output IORQ as an interrupt acknowledge signal that is used to determine the interrupt vector. At this time, when this LSI's CS terminal goes LOW, the LSI may output a WRQ signal and still not be able to capture the vector properly. Therefore, arrange the decoding circuit so that it only functions when the $\overline{M1}$ signal is HIGH.

Note 2: Pull up terminals LD8 to LD15 to the power supply externally (5 to 10 k-ohms).

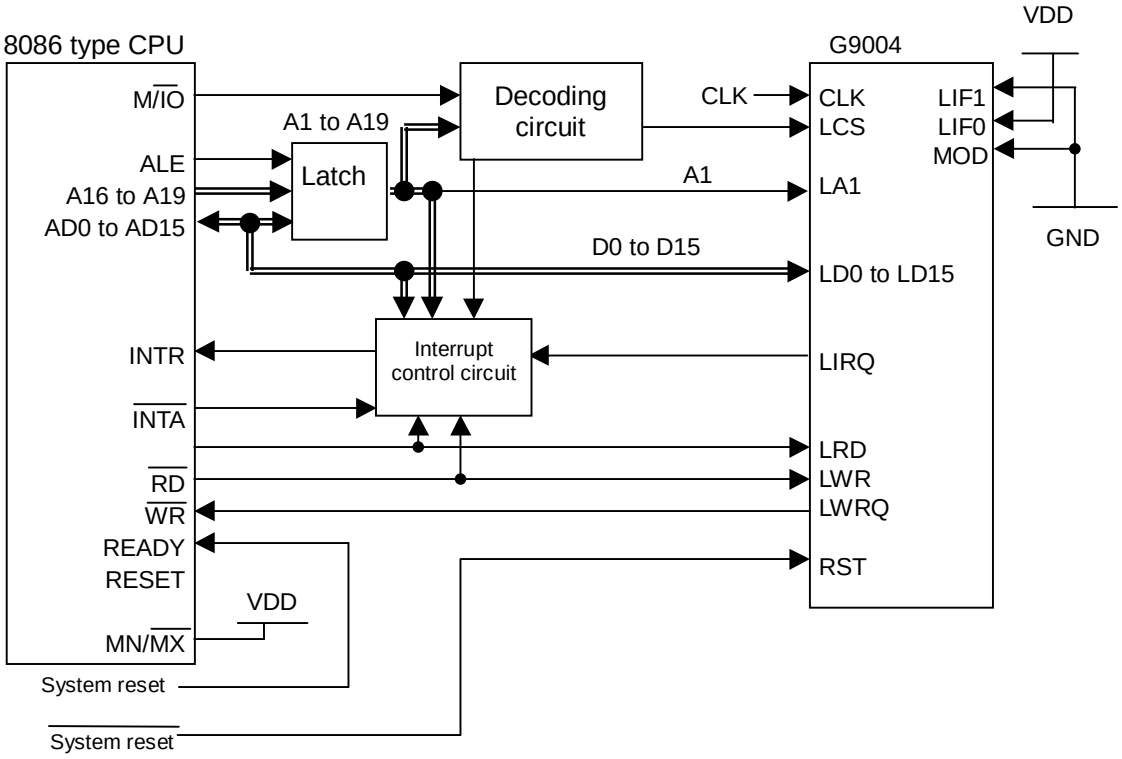
Note 3: Pull the LA2 to LA5 input terminals down to GND using external resistors (5 to 10 K-ohms).

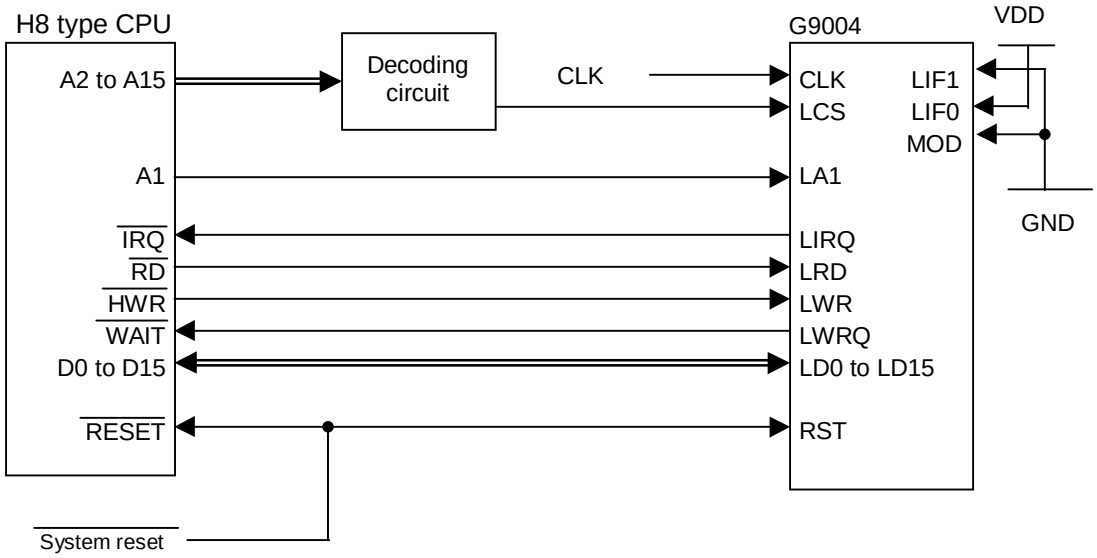
9-1-2. 8-bit I/F (2) (IF1 = HIGH, IF0 = LOW)



Note 1: Pull the LA2 to LA5 terminals down to the GND (5 to 10 K-ohms).
Note 2: Pull the LD8 to LD15 terminals up to the power supply using external resistors (5 to 10 K-ohms).

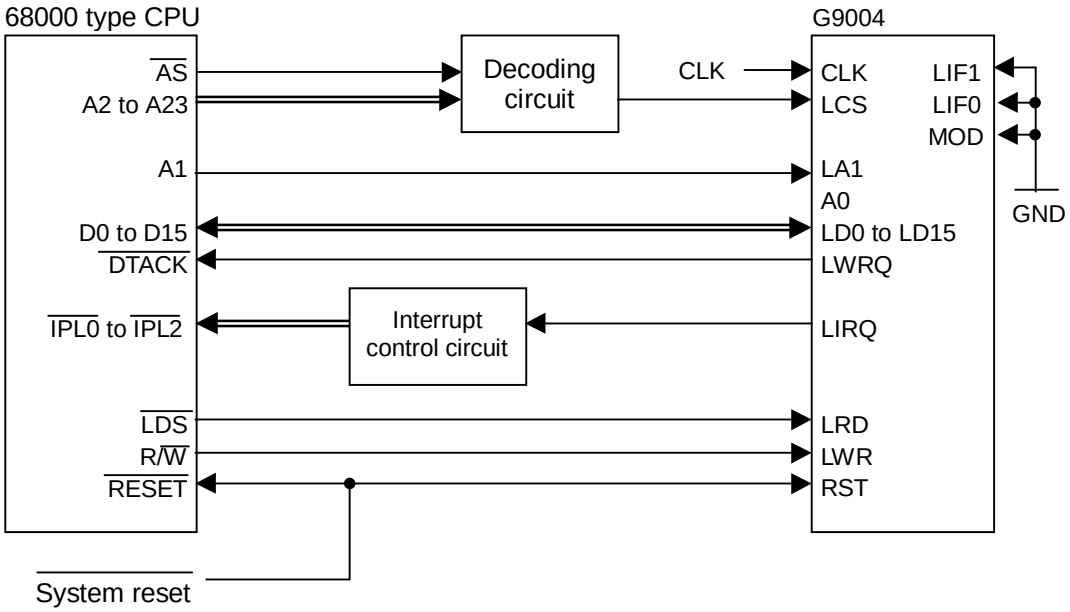
9-1-3. 16-bit I/F (1) (IF1=LOW, IF0=HIGH)





Note 1: Pull LA0, and the LA2 to LA5 terminals down to GND (5 to 10 K-ohms).

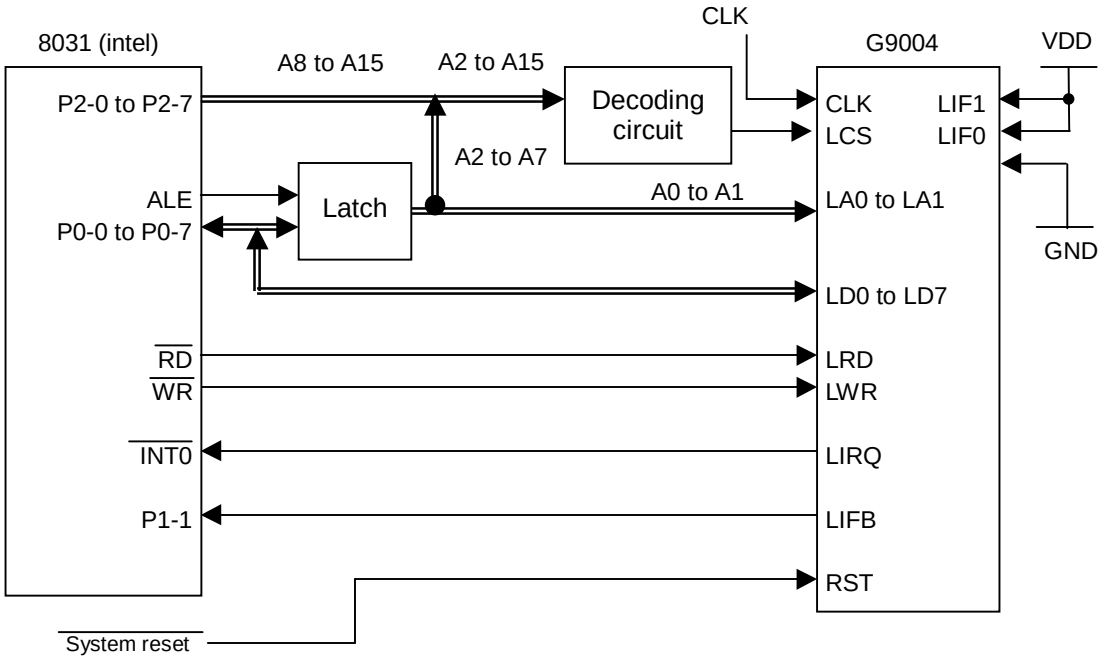
9-1-4. 16-bit I/F (2) (IF1 = LOW, IF0 = LOW)



Note 1: Pull the LA0, LA2 to LA5 input terminals down to GND (5 to 10 K-ohms).

9-1-5. Connecting to a CPU without a wait function

The central device can be connected to a CPU that does not have a wait function.
Let's look at an example with the CPU interface using 8-bit I/F (1) while it is connected to an Intel 8031 8-bit CPU.
Since this CPU does not have a terminal for executing a wait function, care is needed when programming.



[Points]
1) Set IF1 = H and IF0 = H (8-bit I/F (1)).
2) Since the 8031 does not have a wait terminal, the WRQ terminal cannot be used.
However, the G9004 needs a certain internal processing time to access (write/read) a CPU.
And a wait function is therefore essential for continuous access operations.
In the example above, the "LIFB" output terminal on the G9004 is connected to a port on the 8031.
The LIFB bit is monitored using a routine in the 8031, so that the 8031 does not try to access the G9004 while it is processing a command.

Note 1: Pull the LA2 to LA5 terminals down to GND (5~10Kohms).

9-2. Access timing when the CPU message communication mode is selected (MOD = L)

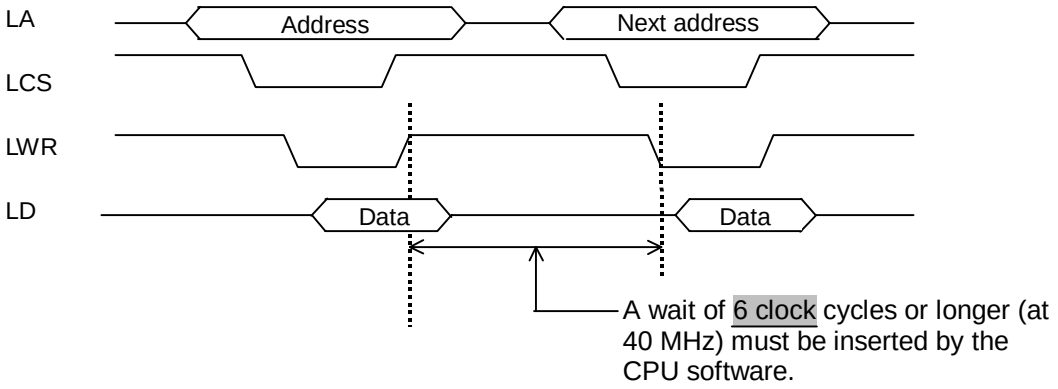
9-2-1. Normal access

CPUs that have a wait function can be connected to the LWRQ terminal on the G9004 so that they can be used without special concern for signal timing.
However, CPUs without a wait function must monitor the LIFB output or use one of the following timing schemes (this is essential).

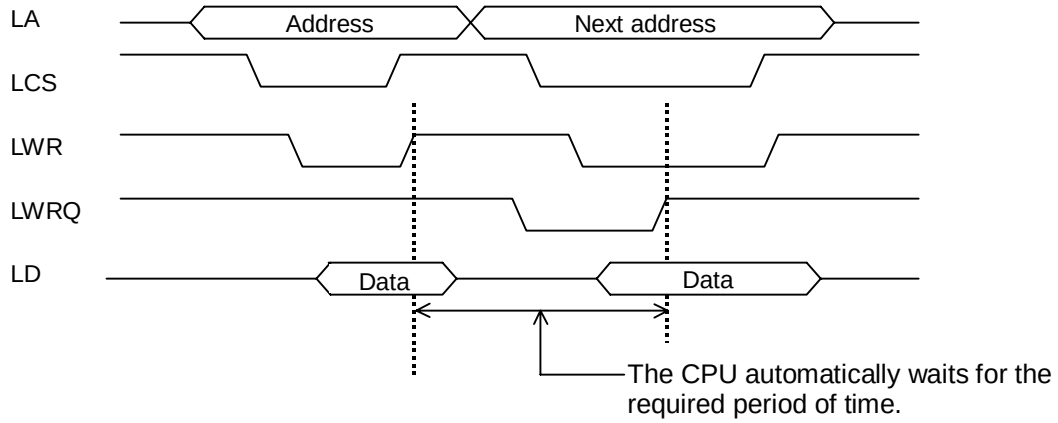
9-2-2. Write to command or data transfer FIFO

The timing for writing to command (address 0 in the 8-bit I/O mode (1)) or the data transfer FIFO (address 2 in the 8-bit I/O mode (1)) is shown below.
A wait time is necessary to perform continuous writing. The wait must be 6 clock cycles or longer at 40 MHz.

1) Does not use the LWRQ output (CPU does not have a wait function)



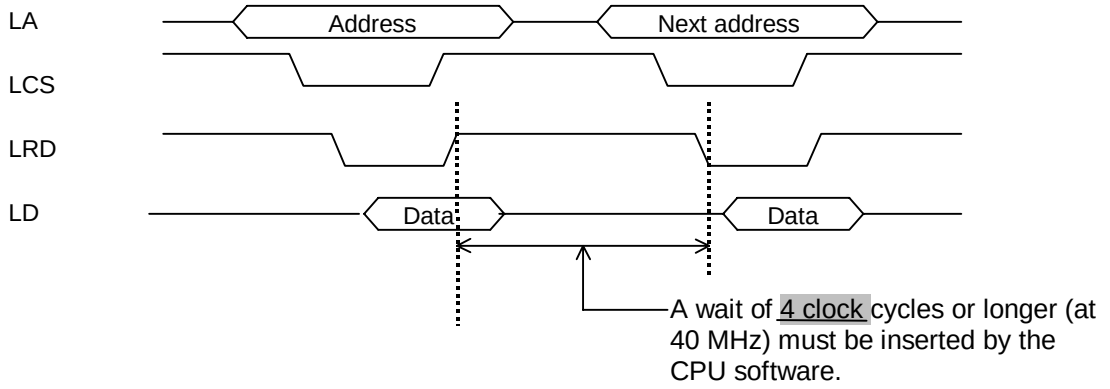
2) Uses the LWRQ output (CPU has a wait function)



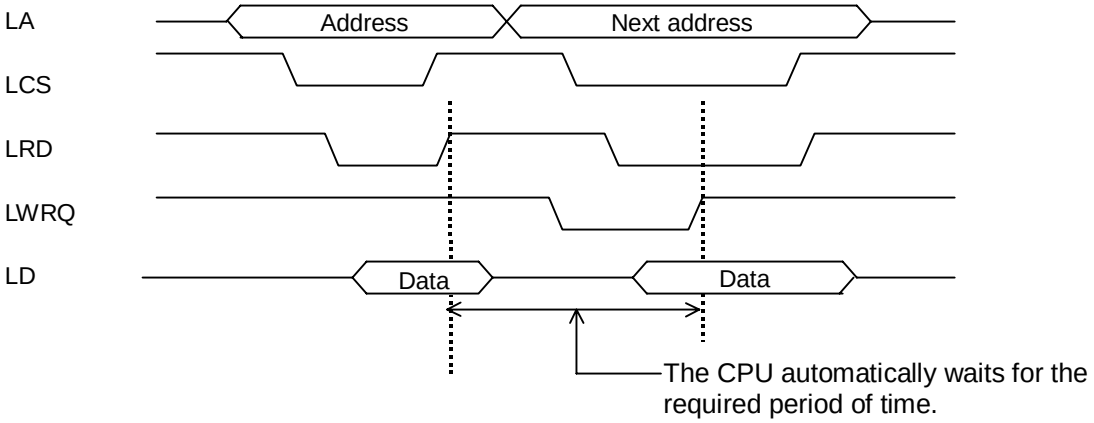
9-2-3. Read status

Shown below is the timing when reading from address 0 in the 8-bit I/O mode (1).
A wait time is necessary to perform continuous writing. The wait must be 4 clock cycles or longer at 40 MHz.

1) Does not use the LWRQ output (CPU does not have a wait function)



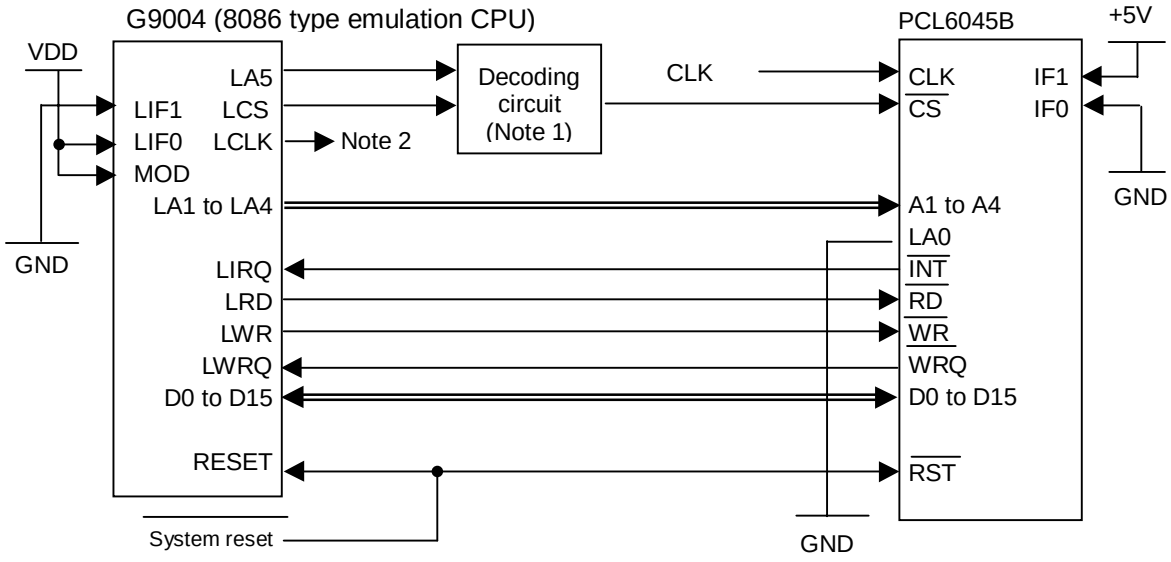
2) Uses the LWRQ output (CPU has a wait function)



9-3. Connection to peripheral LSIs when the CPU emulation mode is selected

9-3-1. Connections to a PCL6045B (8086 type CPU emulation)

The PCL6045B is a pulse train generating LSI for NPM's motion control network. One PCL6045B can generate pulse trains for four axes.

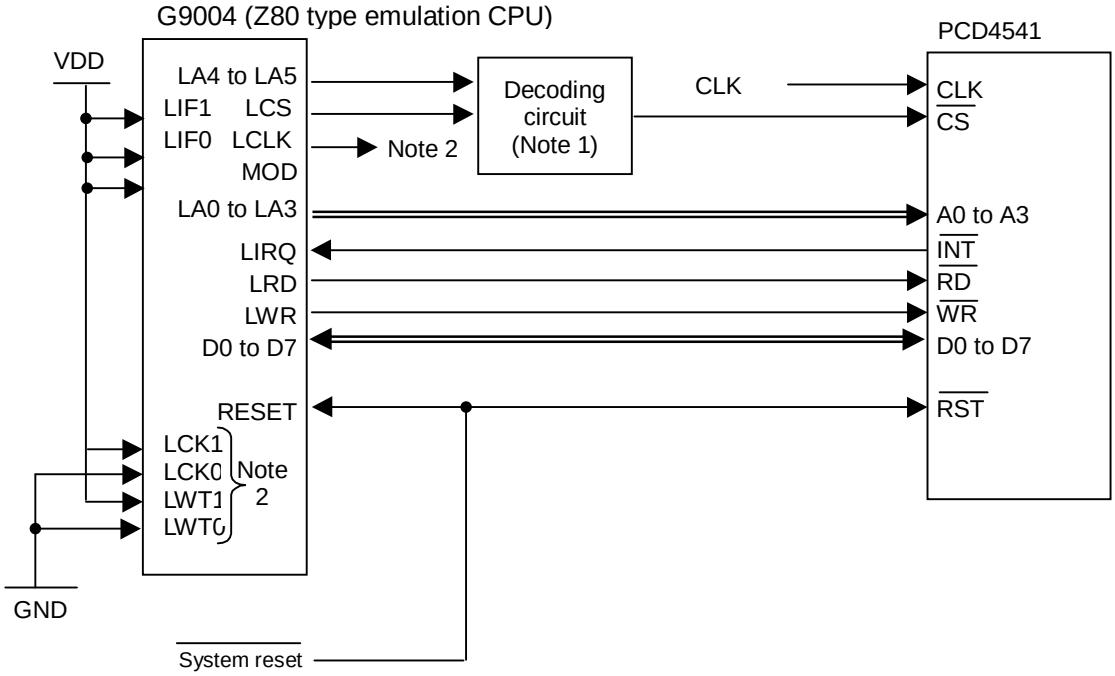


Note 1: The G9004 can be connected to two PCL6045Bs.
In this case, the "LA5" signal is used to tell the two chips apart. This line is the equivalent of a decoder circuit.
When only one device is connected to the G9004, there is no need to provide a decoder circuit. The LCS output terminal on the G9004 can be connected to the $\overline{CS}$ terminal on the PCL6045B.

Note 2: The "LCLK" clock output on the CPU emulation device (G9004) cannot be connected to the CLK input (clock input) on the PCL6045B.
The LCLK output is 3.3 V, but the PCL6045B are 5V devices and their CLK inputs use CMOS levels (V_{IH} = 4 V min., V_{IL} = 1 V max.). They cannot be connected directly to 3.3V devices.
Also, the PCL6045B needs a 19.6608 MHz clock. If it is connected to some other clock speed, such as a 20 MHz clock, it may complicate setting the multiplication factor. For details, see the user's manual for the PCL6045B.

9-3-2. Connections to the PCD4541 (Z80 type CPU emulation)

The PCD4541 is an NPM sequence LSI for use with stepper motors.



Note 1: When only one device is connected to the G9004, there is no need for a decoder circuit. The LCS output terminal on the G9004 can be connected to the $\overline{CS}$ terminal on the PCD4541.

Note 2: The "LCLK" clock output on the CPU emulation device (G9004) cannot be connected to the CLK input (clock input) on the PCD4541.
The LCLK output is 3.3 V, but the PCD4541 is a 5V device and its CLK input uses CMOS levels (V_{IH} = 4 V min., V_{IL} = 1 V max.). It cannot be connected directly to 3.3V devices.
Also, the PCD4541 needs a 4.9152 MHz clock. If it is connected to some other clock speed, such as a 5 MHz clock, it may complicate setting the multiplication factor. For details, see the user's manual for the PCD4541.

Note 3: LCK1 = HIGH, LCK0 = LOW
LWT1 = H, LWT0 = L
When these settings are used, the device will have the status shown below:

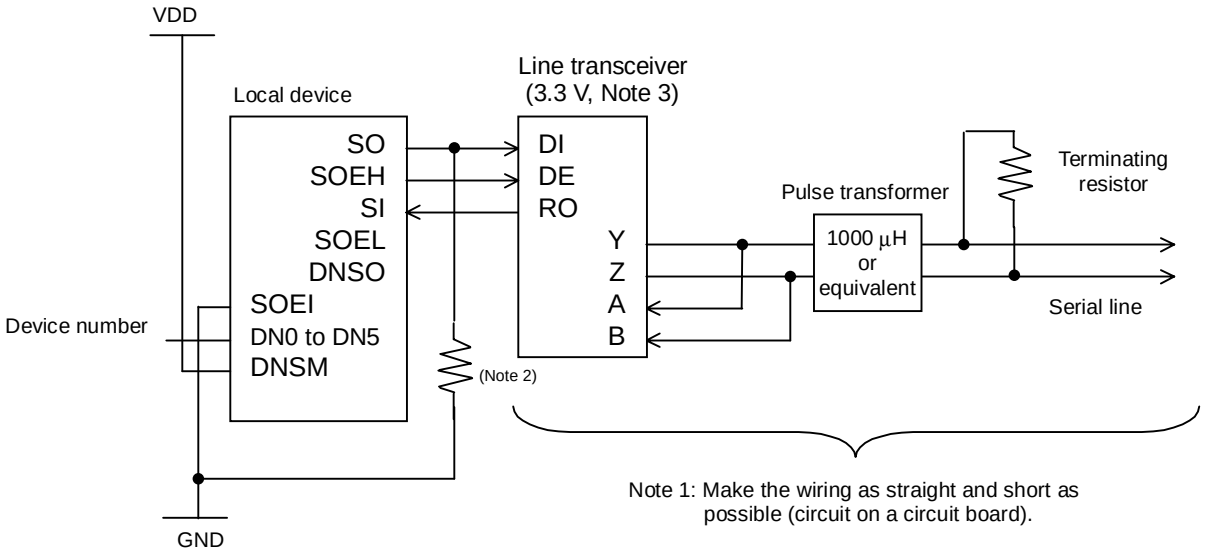
- LCLK = 10 MHz
- Local bus access interval = 5 x T_{LCLK} (500 ns)

The " local bus access interval" is the minimum time from the 1st access to next access, when the CPU emulation device is reading or writing to the PCD4541.
Since the PCD4541 does not have an output terminal to tell a CPU to wait, the CPU has to use its own resources to time the waiting period.
Another method for accessing the PCD4541 is to have the central device (G9001) execute a number of NOP commands to allow the required time to pass. However, using the " local bus access interval" will reduce the burden on the software.
The waiting time of 500 ns was determined from the values specified in the PCD4541 user's manual.

9-4. Connections to a serial communication line

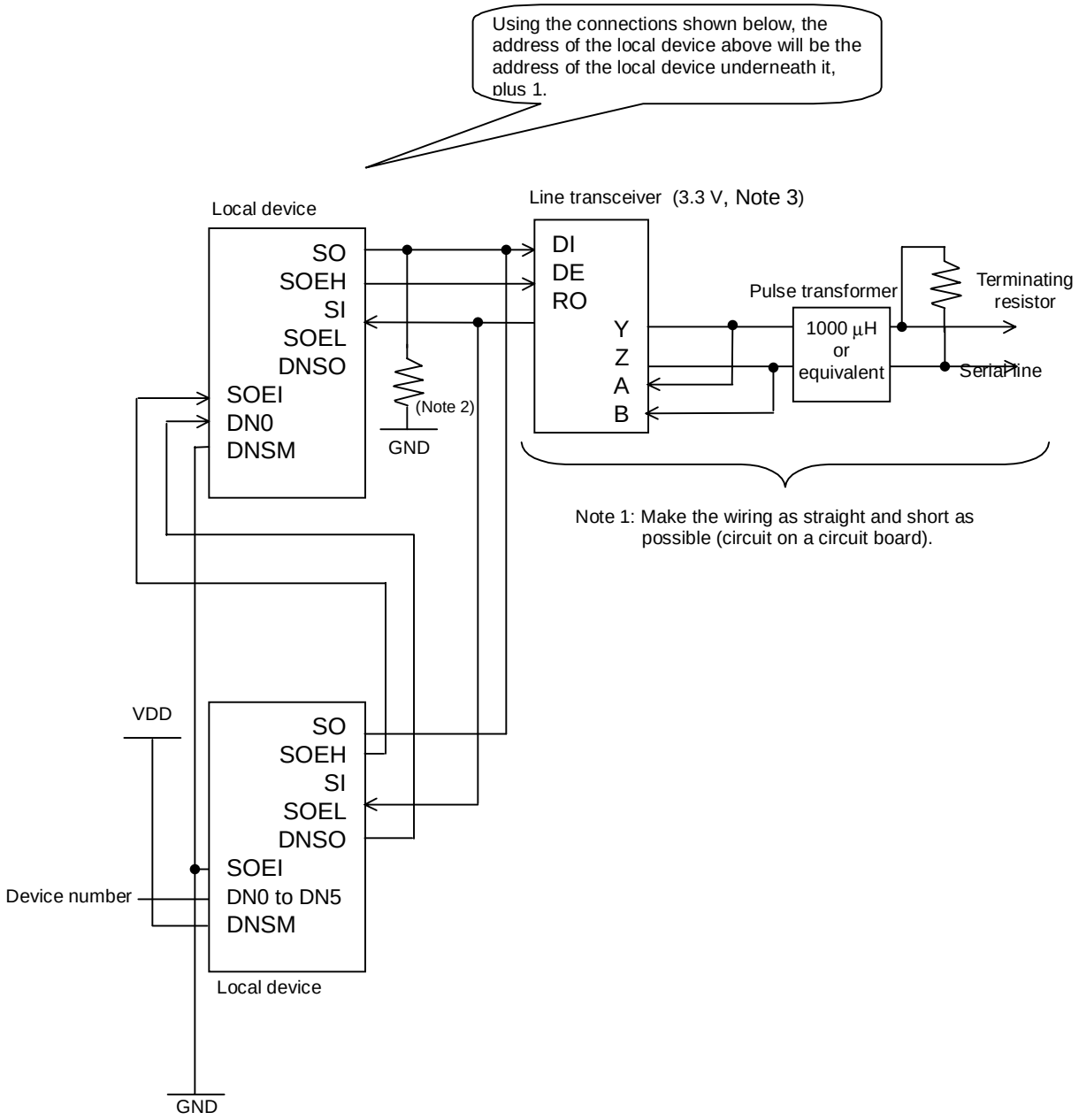
Use RS-485 line transceivers and pulse transformers (1000 □H or equivalent) to make serial communication connections.
Connect the line transceivers as shown below.
Connect terminating resistors (which match the cable impedance) at both ends of the transmission line.
The terminating resistors can be either before or after the pulse transformer. The same effect will be obtained at either position.
When using a 5 V line transceiver, ICs such as a level shifter are needed to assert signals on lines such as "SO," "SOEH," and "SI."

(1) Circuit example for a single local device



Note 1: Make the wiring as straight and short as possible (circuit on a circuit board).

(2) Circuit example for multiple local devices



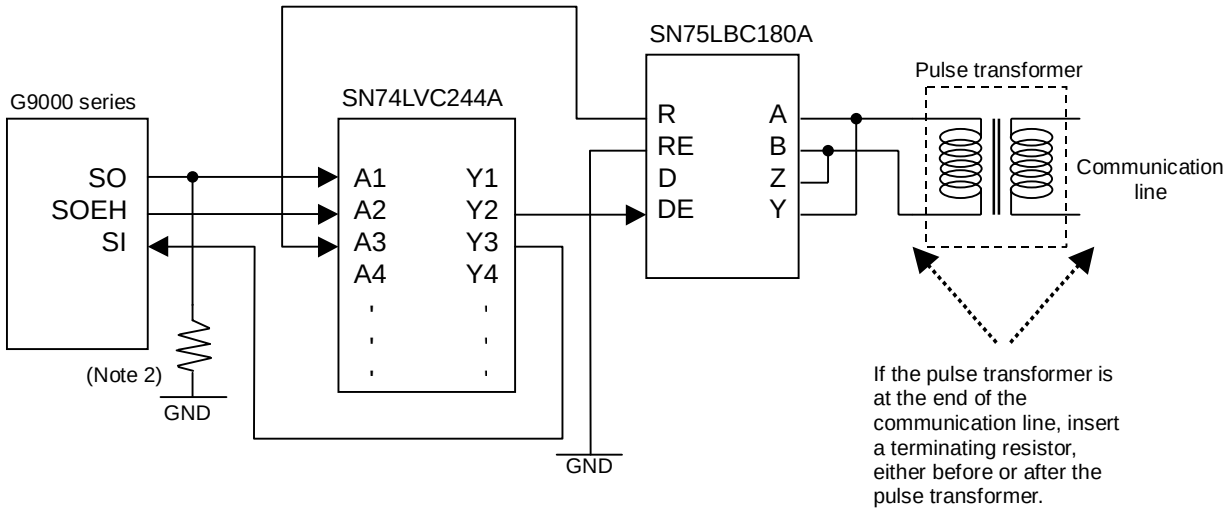
Note 1: When connecting the serial lines to line transceivers, make the path as short and straight as possible.
Running these lines on a PC board could deteriorate the communication performance.

Note 2: Pull down resistors to GND should be 5 to 10 k-ohms.

Note 3: The following ICs can be used as 3.3 V line transceivers.
Ex.: (1) ADM3491AN (DIP) or ADM3491AR (SOIC) made by ANALOG DEVICES Corporation
(2) MAX3362EKA (SOT) made by MAXIM Corporation

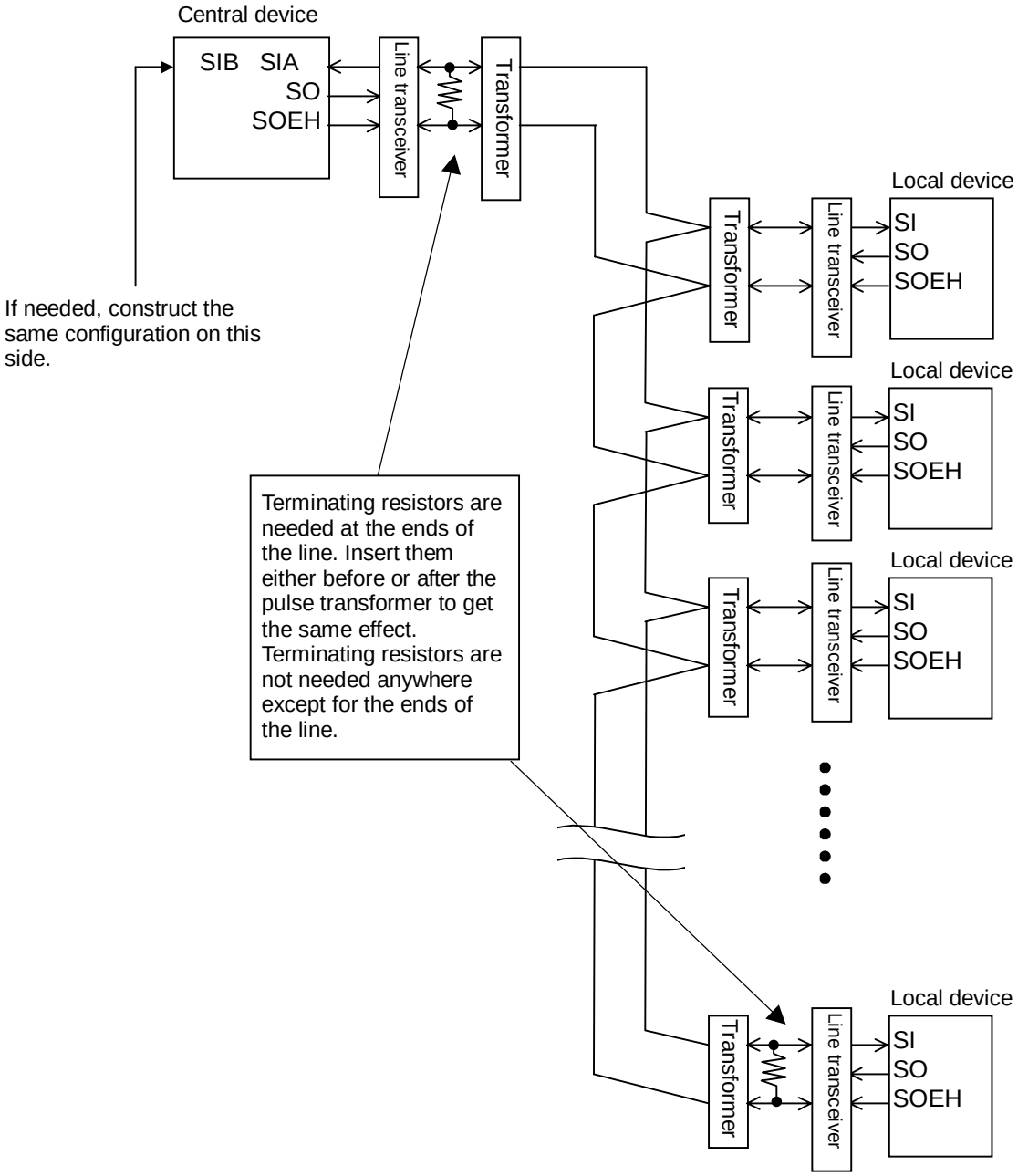
9-5. A connection example of a level shifter

When using a 5 V line transceiver, a level shifter is needed.
Shown below is an example of the connections for a level shifter (TI: SN74LVC244A) and a line transceiver (TI: SN75LBC180A).



9-6. Complete configuration

We recommend a configuration with the central device at one end of the line and the local devices at other end, as shown below.
If you want to place the central device in the middle of the line, use two communication lines so that the central device is effectively at the end of each line.


Central device
SIB
SIA
SO
SOEH
Line transceiver
Transformer
If needed, construct the same configuration on this side.
Terminating resistors are needed at the ends of the line. Insert them either before or after the pulse transformer to get the same effect. Terminating resistors are not needed anywhere except for the ends of the line.
Transformer
Line transceiver
Local device
SI
SO
SOEH

9-7. Recommended environment

Shown below are the results of our experimental communication results and the environment used for the experiment.
These results can be used to design your own system. However, other system configurations are possible. The example below is only for your reference.

Conditions						Results
Transmission rate	Number of local devices	Cable used	Terminating resistor	Pulse transformer	I/F chip	Max. length
20 Mbps	32	CAT5	100 ohm	1000 μH	RS485	100 m
20 Mbps	64	CAT5	100 ohm	1000 μH	RS485	50 m
10 Mbps	64	CAT6	100 ohm	1000 μH	RS485	100 m

Note: In the figures above, the maximum length figures are results from ideal conditions in a laboratory. In actual use, the results may not be the same.

9-7-1. Cable

Commercially available LAN cables were used.
CAT5: Category 5
CAT6: Category 6
We used these LAN cables because they are high quality, inexpensive, and easy to obtain. Lower quality cables (such as cheap instrument cables) may significantly reduce the effective total length of the line. LAN cables normally consist of several pair of wires. Make sure to use wires from the same pair for one set of communication lines.
Even when using cables with the same category and rating, the performance of each cable manufacturer may be different. Always use the highest quality cables in the same category.

9-7-2. Terminating resistor

Select resistors that match the impedance of the cable used.
Normally, a 100 ohm resistor is recommended. Therefore, we used terminating resistors with this value.
Adjusting this resistor value may improve the transmission line quality.

9-7-3. Pulse transformer

We recommend using pulse transformers, in order to isolate the GND of each local device.
By isolating the GNDs, the system will have greater resistance to electrical noise. If pulse transformers are not used, the transmission distance may be less.
We used 1000 □H transformers in our experiments.

9-7-4. I/F chip

We selected I/C chips with specifications better than the RS485 standard.
In the experiment, we used 5 V line transceivers. When 5 V line transceivers are used, level shifters are needed to make the connections.

9-7-5. Parts used in our experiments

Show below is a list of the parts used in the interface circuits of our experiments.
Use of other parts may change the system's response. This list is only for your reference.

Parts	Manufacturer	Model name
CAT5	Oki Wire Co., Ltd.	F-DTI-C5 (SLA)
CAT6	Oki Wire Co., Ltd.	DTI-C6X
Pulse transformer	JBC Co., Ltd.	DP101-102F
Line transceiver	TEXAS INSTRUMENTS	SN75LBC180AP
Level shifter	TEXAS INSTRUMENTS	SN74LVC244ADB

9-7-6. Other precautions

- Cables
  When you are planning long distance transmission, cable quality will be the single most important factor.
  Specialized cables designed for use as field busses, such as those by CC-Link and LONWORKS, have guaranteed quality and may be easier to use.

- Pulse transformers
  Needless to say, the pulse transformers should handle 20 Mbps (10 MHz) without becoming saturated. The transformer's inductance is also important.
  Since up to 64 pulse transformers may be connected, the actual working specifications of these devices must be very similar.
  We used 1000 μH pulse transformers. However, in order to obtain better response characteristics, you may want to try pulse transformers with a larger reactance.

- Line transceivers
  We used TEXAS Instruments chips for the experiments.
  Other possibilities are available from MAXIM and LINEAR TECHNOLOGY, who offer very high performance transceivers.

- Connectors
  If possible, the connectors should match the cable characteristics.
  Although we did not use them, modular type connecters will be better for LAN cables.

- Cable connections
  Do not connect one cable to another cable (using connectors etc.).
  In a multi-drop system, the number of cables increases as the number of local devices increase. However, connecting a cable just to extend the line should be avoided.

- Processing of excess cable
  Excess cable, left over after making all the runs, should be eliminated.
  Unneeded cable length may restrict the line overall usable length, and may introduce electrical noise.

- Circuit board substrate
  Create circuits on a substrate with 4 or more layers, to prevent the introduction of noise.

- Estimating cable length in the system design phase
  In the first estimate, use shorter line lengths. In the actual system configuration, lines may be lengthened. Estimates made using the maximum length may lead to impossible communication distances.

- Minimum cable length
  Each cable must be at least 60 cm long. Although this may seem contradictory to the excess cable precaution, this minimum length is necessary.

- Using different cables in one system
  Do not mix cables from different manufacturers, even when they are in the same category.
  (Different cable models from the same manufacturer should not be used either.)
  Using different cables together may deteriorate the communication quality.

10. Center device (G9001)

We will use the following four commands to access the address map in the central device.

1) Write command to the central device (16 bits)

Outpw (Address, Data)	
Address	Value corresponding to the address map in the central device (16 bits). The lowest bit is ignored.
Data	Data to write (16 bits)
Return value	None

2) Write command to the central device (8 bits)

Outp (Address, Data)	
Address	Value corresponding to the address map in the central device (16 bits).
Data	Data to write (8 bits)
Return value	None

3) Read command from the central device (16 bits)

Inpw (Address)	
Address	Value corresponding to the address map in the central device (16 bits). The lowest bit is ignored.
Return value	Read data (16 bits)

4) Read command from the central device (8 bits)

Inpw (Address)	
Address	Value corresponding to the address map in the central device (16 bits).
Return value	Read data (8 bits)

Also, see the individual items in the "Message communication procedure" and "CPU emulation procedure" sections.

10-1. Program example of the CPU emulation mode

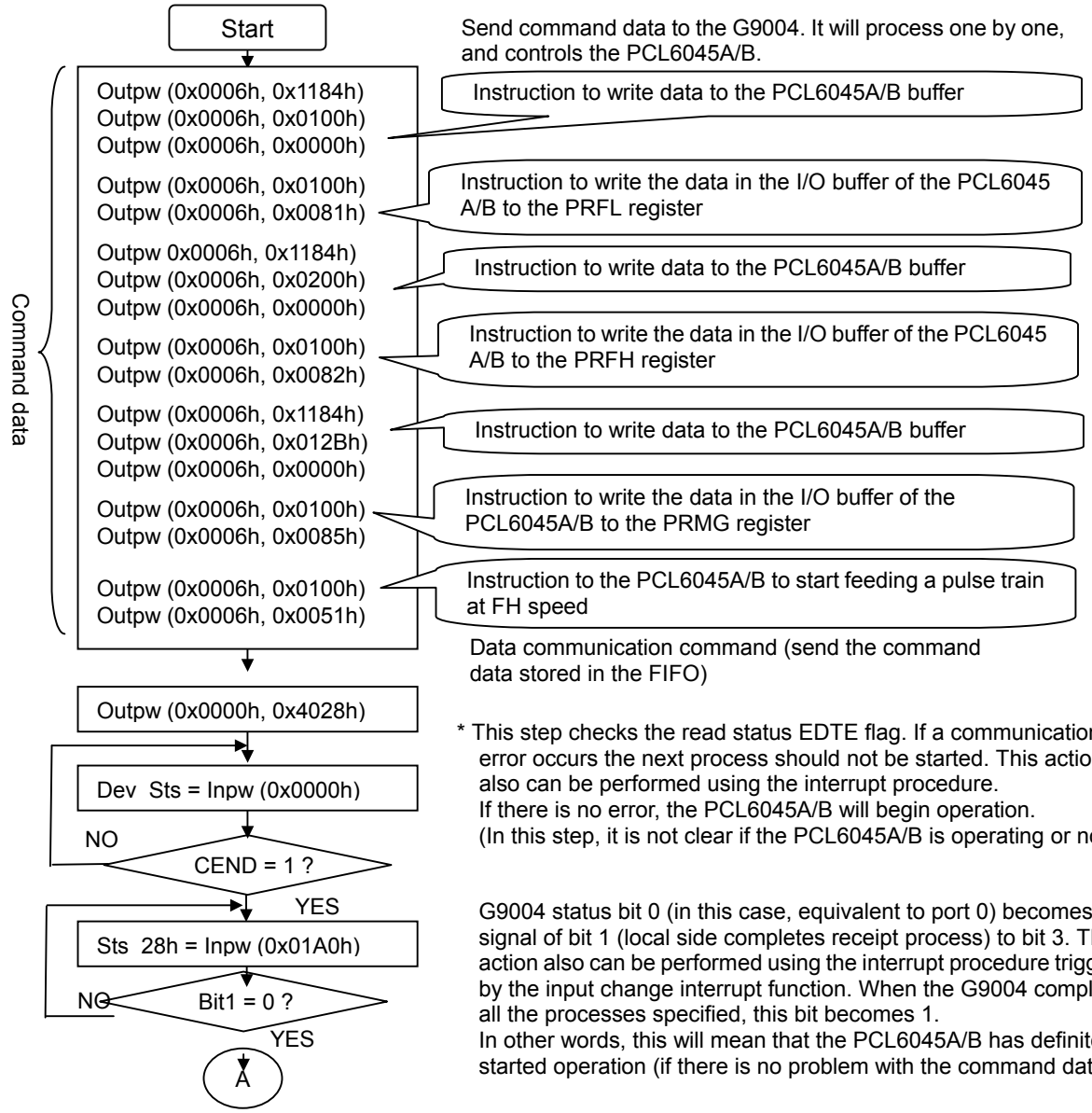
Using the CPU interface mode of the G9004, the PCL6045A/B uses a 16-bit I/F (1), and the PCD4541 uses an 8-bit I/F (1).

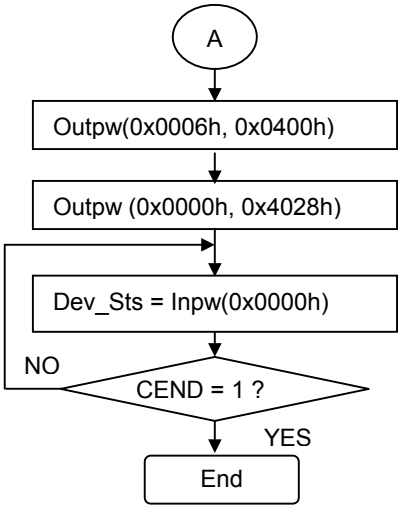
10-1-1. Control example of the PCL6045A/B

Shown below is a program example that lets the central device (G9001) control a PCL6045A/B through a G9004.
The PCL6045A/B is a pulse train generating LSI for NPM's motion control network. Set the CPU-I/F to 8086 mode (IF0 = L, IF1 = H).
One PCL6045A/B can generate pulse trains for four axes.
In the example below, use the device address of "28h" for the G9004.

Registers to set in the PCL6045A/B

Register name	Set value	Remark
PRFL	00000100h	
PRFH	00000200h	
PRMG	012Bh	Multiplication rate = 1


Start
Command data
Outpw (0x0006h, 0x1184h)
Outpw (0x0006h, 0x0100h)
Outpw (0x0006h, 0x0000h)
Outpw (0x0006h, 0x0100h)
Outpw (0x0006h, 0x0081h)
Outpw 0x0006h, 0x1184h)
Outpw (0x0006h, 0x0200h)
Outpw (0x0006h, 0x0000h)
Outpw (0x0006h, 0x0100h)
Outpw (0x0006h, 0x0082h)
Outpw (0x0006h, 0x1184h)
Outpw (0x0006h, 0x012Bh)
Outpw (0x0006h, 0x0000h)
Outpw (0x0006h, 0x0100h)
Outpw (0x0006h, 0x0085h)
Outpw (0x0006h, 0x0100h)
Outpw (0x0006h, 0x0051h)
Outpw (0x0000h, 0x4028h)
Dev Sts = Inpw (0x0000h)
NO
CEND = 1 ?
YES
Sts 28h = Inpw (0x01A0h)
NO
Bit1 = 0 ?
YES
A
Send command data to the G9004. It will process one by one, and controls the PCL6045A/B.
Instruction to write data to the PCL6045A/B buffer
Instruction to write the data in the I/O buffer of the PCL6045 A/B to the PRFL register
Instruction to write data to the PCL6045A/B buffer
Instruction to write the data in the I/O buffer of the PCL6045 A/B to the PRFH register
Instruction to write data to the PCL6045A/B buffer
Instruction to write the data in the I/O buffer of the PCL6045A/B to the PRMG register
Instruction to the PCL6045A/B to start feeding a pulse train at FH speed
Data communication command (send the command data stored in the FIFO)
* This step checks the read status EDTE flag. If a communication error occurs the next process should not be started. This action also can be performed using the interrupt procedure.
If there is no error, the PCL6045A/B will begin operation.
(In this step, it is not clear if the PCL6045A/B is operating or not.)
G9004 status bit 0 (in this case, equivalent to port 0) becomes OR signal of bit 1 (local side completes receipt process) to bit 3. This action also can be performed using the interrupt procedure triggered by the input change interrupt function. When the G9004 completes all the processes specified, this bit becomes 1.
In other words, this will mean that the PCL6045A/B has definitely started operation (if there is no problem with the command data).



Put a reset instruction command for the " local receive processing complete " flag in the FIFO.

Write a data communication command (send the command data written in the FIFO)

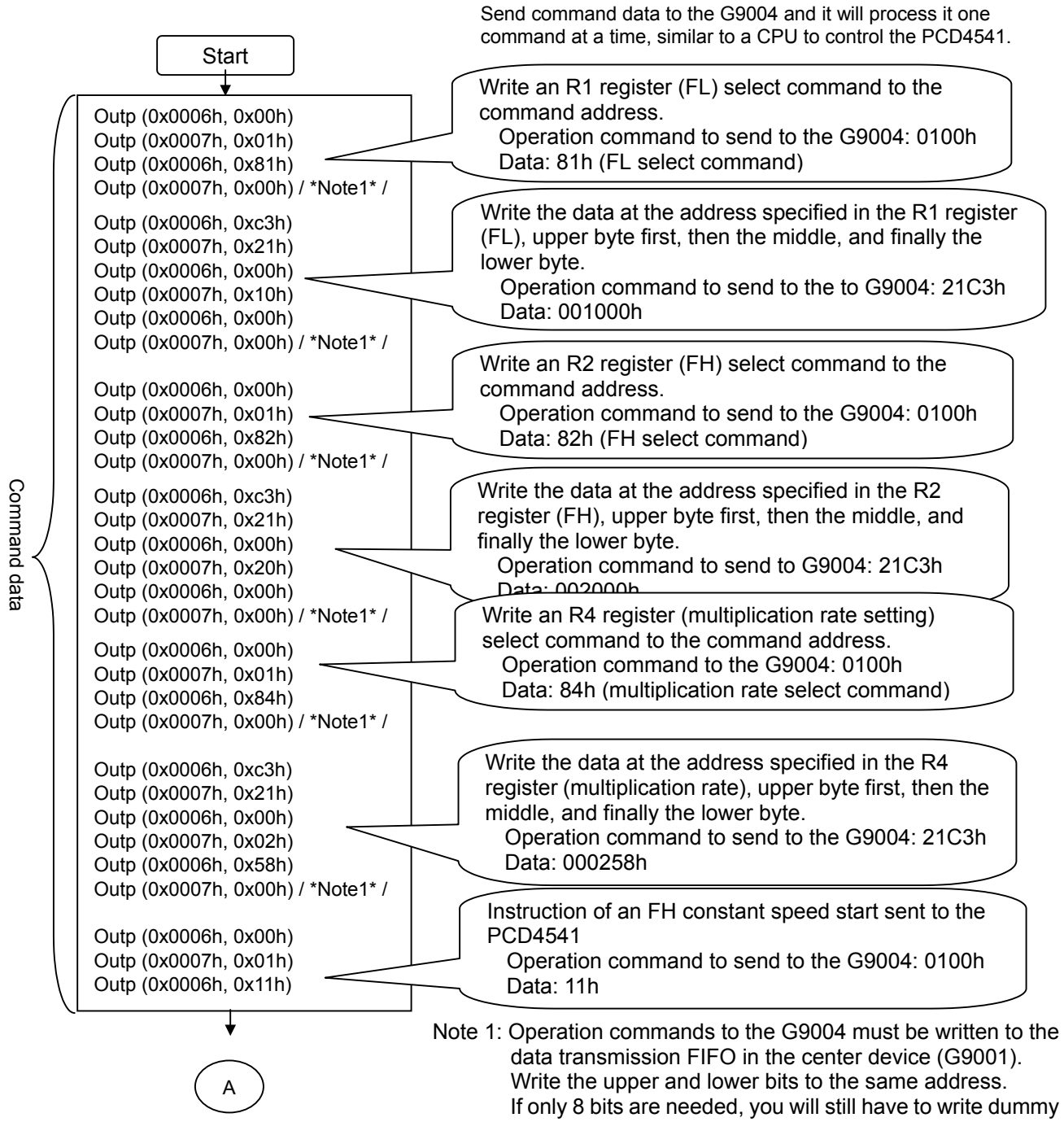
When CEND = H, the local device flag has been reset.

10-1-2. Control example of PCD4541

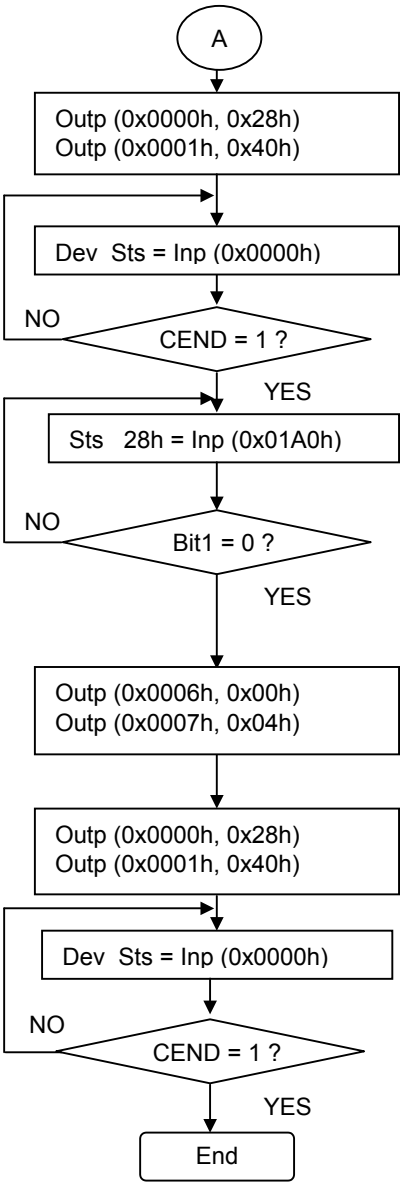
Below shows a program example that lets a central device (G9001) control a PCD4541 through a G9004. In this example, the central device (G9001) communicates in CPU-I/F model 4 (Z80 type 8-bit CPU). The PCD4541 is NPM's sequence LSI for stepper motors. In the example below, use a device address of "28h" for the G9004.

Registers to set in the PCD4541

Register name	Set value	Remark
PRFL	001000h	
PRFH	002000h	
PRMG	000258h	Multiplication rate = 1


Send command data to the G9004 and it will process it one command at a time, similar to a CPU to control the PCD4541.
Start
Command data
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x01h)
Outp (0x0006h, 0x81h)
Outp (0x0007h, 0x00h) / *Note1* /
Write an R1 register (FL) select command to the command address.
Operation command to send to the G9004: 0100h
Data: 81h (FL select command)
Outp (0x0006h, 0xc3h)
Outp (0x0007h, 0x21h)
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x10h)
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x00h) / *Note1* /
Write the data at the address specified in the R1 register (FL), upper byte first, then the middle, and finally the lower byte.
Operation command to send to the to G9004: 21C3h
Data: 001000h
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x01h)
Outp (0x0006h, 0x82h)
Outp (0x0007h, 0x00h) / *Note1* /
Write an R2 register (FH) select command to the command address.
Operation command to send to the G9004: 0100h
Data: 82h (FH select command)
Outp (0x0006h, 0xc3h)
Outp (0x0007h, 0x21h)
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x20h)
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x00h) / *Note1* /
Write the data at the address specified in the R2 register (FH), upper byte first, then the middle, and finally the lower byte.
Operation command to send to G9004: 21C3h
Data: 002000h
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x01h)
Outp (0x0006h, 0x84h)
Outp (0x0007h, 0x00h) / *Note1* /
Write an R4 register (multiplication rate setting) select command to the command address.
Operation command to the G9004: 0100h
Data: 84h (multiplication rate select command)
Outp (0x0006h, 0xc3h)
Outp (0x0007h, 0x21h)
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x02h)
Outp (0x0006h, 0x58h)
Outp (0x0007h, 0x00h) / *Note1* /
Write the data at the address specified in the R4 register (multiplication rate), upper byte first, then the middle, and finally the lower byte.
Operation command to send to the G9004: 21C3h
Data: 000258h
Outp (0x0006h, 0x00h)
Outp (0x0007h, 0x01h)
Outp (0x0006h, 0x11h)
Instruction of an FH constant speed start sent to the PCD4541
Operation command to send to the G9004: 0100h
Data: 11h
A

Note 1: Operation commands to the G9004 must be written to the data transmission FIFO in the center device (G9001). Write the upper and lower bits to the same address. If only 8 bits are needed, you will still have to write dummy data to upper 8 bits, and sent an operation command to the G9004 using the same address.



Data communication command (send the command data stored in the FIFO)
Write in order of lower to upper bit.

* This step checks the read status EDTE flag. If a communication error occurs the next process should not be started. This action also can be performed using the interrupt procedure.
If there is no error, the PCD4541 will begin operation.
(In this step, it is not clear if the PCD4541 is operating or not.)

- G9004 status bit 1 (in this case, equivalent to port 0) indicates whether reception by the local devices is complete. This action also can be performed using the interrupt procedure triggered by the input change interrupt function. When the G9004 completes all the processes specified, this bit becomes 1. In other words, this will mean that the PCD4541 has definitely started operation (if there is no problem with the command data).

Put a reset instruction command for the " local receive processing complete " flag in the FIFO.

Write a data communication command (send the command data stored in the FIFO)

When CEND = H, the local device flag has been reset.

11. Electrical Characteristics

11-1. Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	V_{SS} -0.3 to +4.0	V
Input voltage	V_{IN}	V_{SS} -0.3 to V_{DD} +0.5	V
Input voltage (5V-I/F)	V_{IN}	V_{SS} -0.3 to +7.0	V
Output current / Terminal	I_{OUT}	±30	mA
Storage temperature	T_{STO}	-65 to +150	°C

11-2. Recommended operating conditions

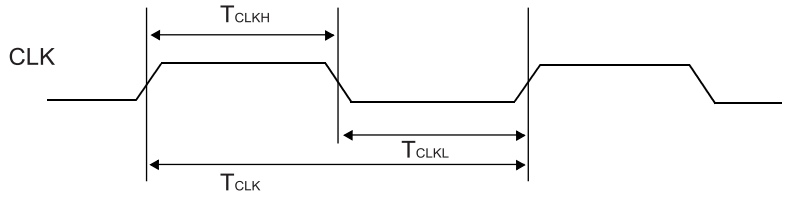
Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	+0.3±10%	V
Input voltage	V_{IN}	V_{SS} to V_{DD}	V
Input voltage (5V-I/F)	V_{IN}	V_{SS} to +5.5	V
Storage temperature	T_a	-40 to +85	°C

11-3. DC characteristics

Item	Symbol	Condition	Min.	Max.	Unit
Current consumption	I_{dd}	CLK = 80 MHz		34	mA
Input leakage current	I_{LI}		-1	1	µA
Output leakage current	I_{OZ}		-1	1	µA
Input capacitance				10	pF
LOW input current	I_{IL}	DN0 to 5, DNSM, SPD0 to 1, TUD, TMD, LCK0 to 1, LIFO 0 to 1, LWT0 to 1, CKSL, MOD	-165		µA
		Input terminals and input/output terminals other than the above.	-1		µA
HIGH input current	I_{HL}	SOEI, SI, BRK		190	µA
		Input terminals and input/output terminals other than the above.	-1	1	µA
LOW input current	V_{IL}			0.8	V
HIGH input current	V_{IH}		2.0		V
LOW output voltage	V_{OL}	I_{OL} = 6 mA		0.4	V
HIGH output voltage	V_{OH}	I_{OH} = -6 mA	V_{DD}-0.4		V
LOW output current	I_{OL}	V_{OL} = 0.4 V		6	mA
HIGH output current	I_{OH}	V_{OH} = V_{DD} -0.4 V	-6		mA
Internal pull up, pull down resistance	R_{Pud}		20	120	K-ohm

11-4. AC characteristics

11-4-1. System clock



1) When setting CKSL = L and data transfer rate = 20 Mbps

Item	Symbol	Min.	Max.	Unit
Frequency	f_{CLK}	-	40	MHz
Cycle	T_{CLK}	25		ns
HIGH duration	T_{CLKH}	10	15	ns
LOW duration	T_{CLKL}	10	15	ns

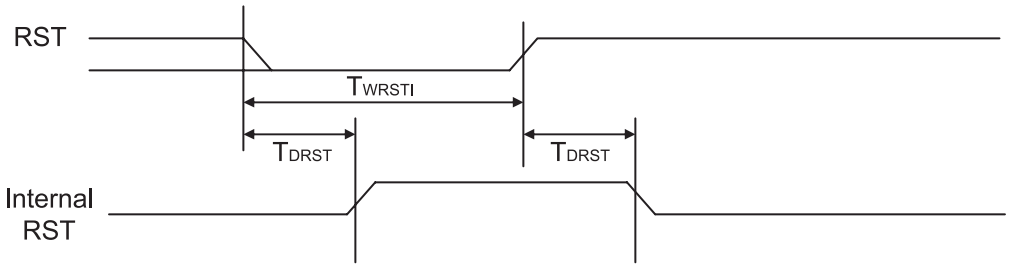
2) When setting CKSL = L and data transfer rate = 10 Mbps

Item	Symbol	Min.	Max.	Unit
Frequency	f_{CLK}	-	40	MHz
Cycle	T_{CLK}	25		ns
HIGH duration	T_{CLKH}	-	-	ns
LOW duration	T_{CLKL}	-	-	ns

3) When setting CKSL = H

Item	Symbol	Min.	Max.	Unit
Frequency	f_{CLK}	-	80	MHz
Cycle	T_{CLK}	-	12.5	ns
HIGH duration	T_{CLKH}	-	-	ns
LOW duration	T_{CLKL}	-	-	ns

11-4-2. Reset timing



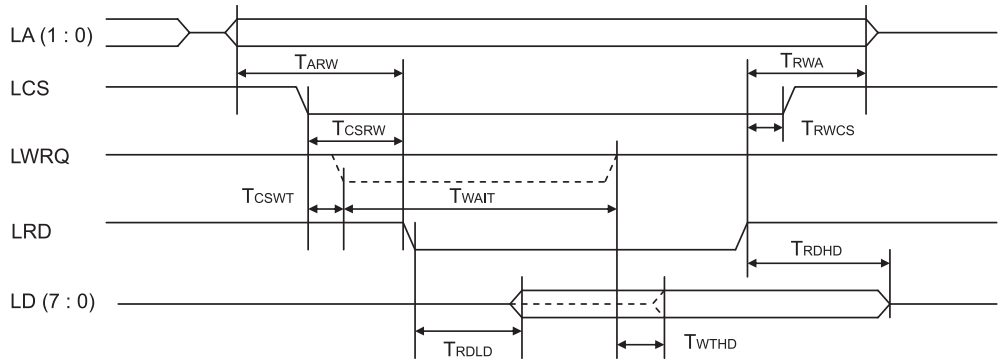
Item	Symbol	Min.	Max.	Unit
Reset length	T_{WRSTI}	10	-	Clock cycles
Delay time	T_{DRST}	-	10	Clock cycles

Note 1: The reset signal must last at least 10 cycles of the system clock.
While resetting, make sure the clock signal is continuously available to the device.
If the clock is stopped while resetting, the device cannot be reset normally.

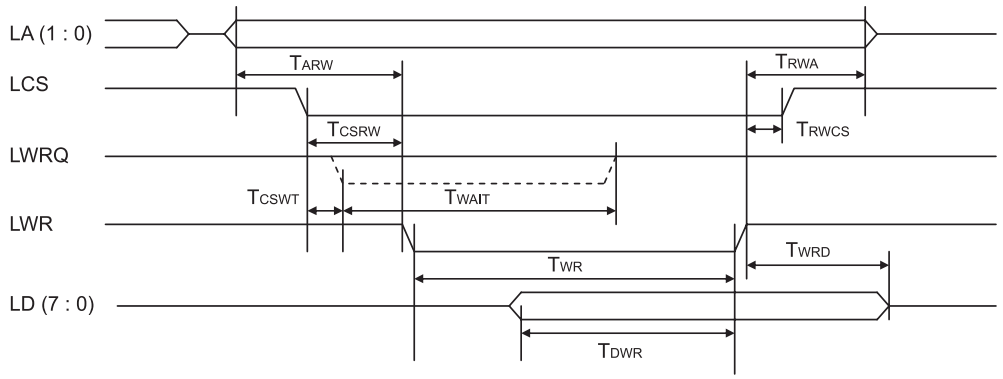
11-5. Timing of CPU message communication mode

11-5-1. 8-bit I/F (1) (IF1 = H, IF0 = H)

- Read cycle



- Write cycle

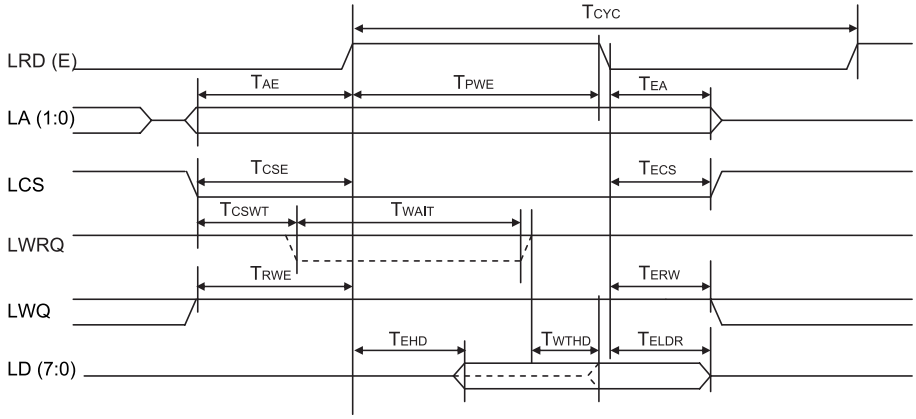


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LRD, LWR ↓	T_{ARW}		17		ns
Address hold time for LRD, LWR ↑	T_{RWA}		0		ns
LCS setup time for LRD, LWR ↓	T_{CSRW}		5		ns
LCS hold time for LRD, LWR ↑	T_{RWCS}		0		ns
LWRQ=ON delay time for LCS ↓	T_{CSWT}	C_L = 40pF		12	ns
LWRQ signal LOW time	T_{WAIT}	Note 1		$6T_{CLK}$ +11	ns
Data output delay time for LRD ↓	T_{RDLD}	C_L = 40pF		29	ns
Data output delay time for LWRQ ↑	T_{WTHD}	C_L = 40pF		16	ns
Data float delay time for LRD ↑	T_{RDHD}	C_L = 40pF		30	ns
LWR signal width	T_{WR}	Note 2	12		ns
Data setup time for LWR ↑	T_{DWR}		22		ns
Data hold time for LWR ↑	T_{WRD}		0		ns

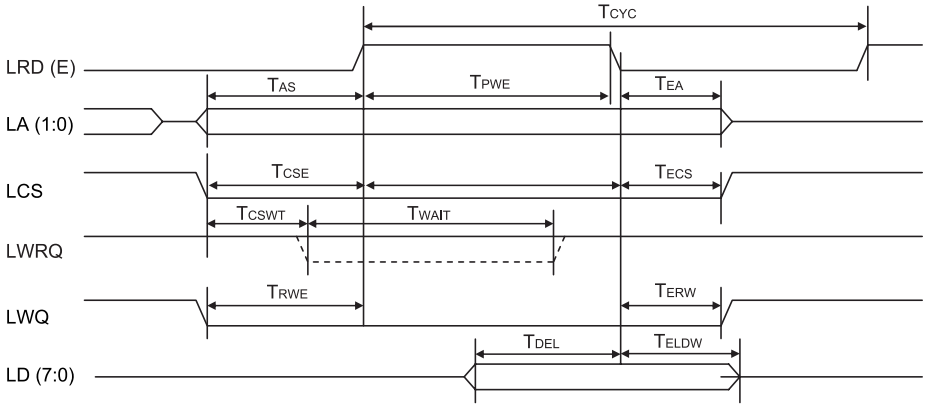
Note1: When CKSL = LOW or CKSL = HIGH, the data output delay time will be 12 T_{CLK} + 11.
Note 2: The time that the WRQ signal is output will be the interval after WRQ goes HIGH until WR goes HIGH.

11-5-2. 8-bit I/F (2) (IF1 = H, IF0 = L)

- Read cycle



- Write cycle

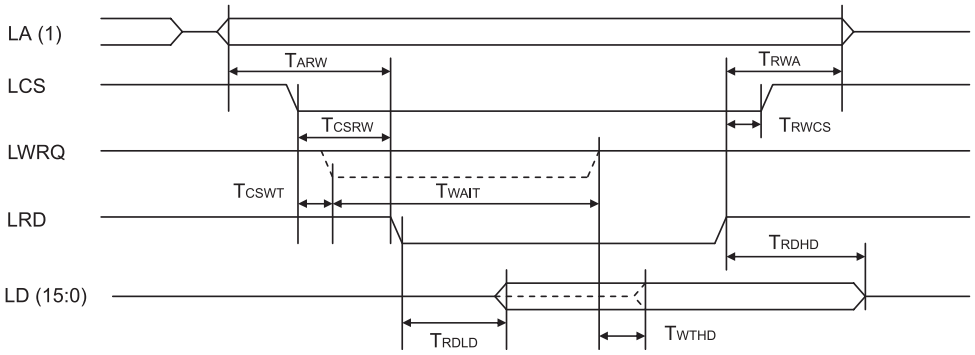


Item	Symbol	Condition	Min.	Max.	Unit
Enable cycle time	T_{CYC}		100		ns
Enable pulse width	T_{PWE}		40		ns
Address setup time for LRD (E) ↑	T_{AE}		17		ns
Address hold time for LRD (E) ↓	T_{EA}		0		ns
R/W setup time for LRD (E) ↑	T_{RWE}		5		ns
R/W hold time for LRD (E) ↓	T_{ERW}		5		ns
LCS setup time for LRD (E) ↑	T_{CSE}		5		ns
LCS hold time for LRD (E) ↓	T_{ECS}		0		ns
LWRQ=ON delay time for LCS ↓	T_{CSWT}	C_L = 40pF		12	ns
LWRQ signal LOW time	T_{WAIT}	Note 1		$6T_{CLK}$+11	ns
Data output delay time for LRD (E) ↑	T_{EHD}	C_L = 40pF		19	ns
Data output delay time for LWRQ ↑	T_{WTHD}	C_L = 40pF		6	ns
Data float delay time for LRD (E) ↓	T_{ELDR}	C_L = 40pF		19	ns
Data setup time for LRD (E) ↓	T_{DEL}		22		ns
Data hold time for LRD (E) ↓	T_{ELDW}		0		ns

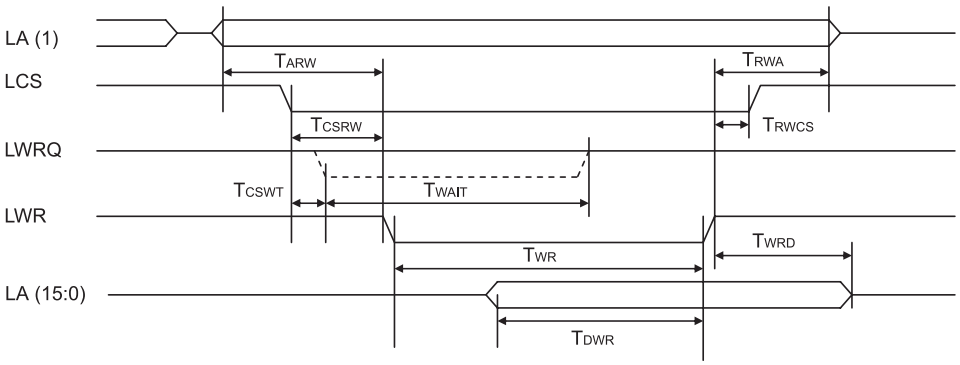
Note 1: When CKSL = LOW or CKSL = HIGH, the data output delay time will be 12 T_{CLK} + 11.

11-5-3. 16-bit I/F (1) (IF1 = L, IF0 = H)

- Read cycle



- Write cycle

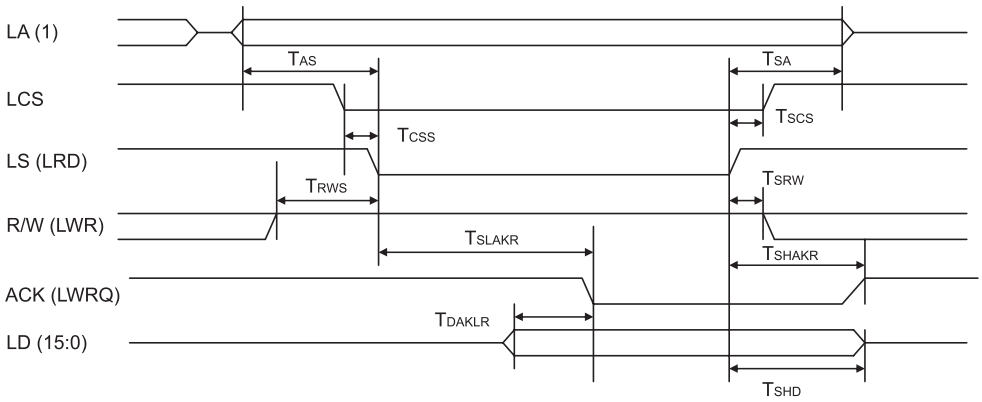


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LRD, LWR ↓	T_{ARW}		17		ns
Address hold time for LRD, LWR ↑	T_{RWA}		0		ns
LCS setup time for LRD, LWR ↓	T_{CSRW}		5		ns
LCS hold time for LRD, LWR ↑	T_{RWCS}		0		ns
LWRQ=ON delay time for LCS ↓	T_{CSWT}	C_L = 40pF		12	ns
LWRQ signal LOW time	T_{WAIT}	Note 1		$6T_{CLK}$ +11	ns
Data output delay time for LRD ↓	T_{RDLD}	C_L = 40pF		29	ns
Data output delay time for LWRQ ↑	T_{WTHD}	C_L = 40pF		16	ns
Data float delay time for LRD ↑	T_{RDHD}	C_L = 40pF		30	ns
LWR signal width	T_{WR}	Note 2	12		ns
Data setup time for LWR ↑	T_{DWR}		22		ns
Data hold time for LWR ↑	T_{WRD}		0		ns

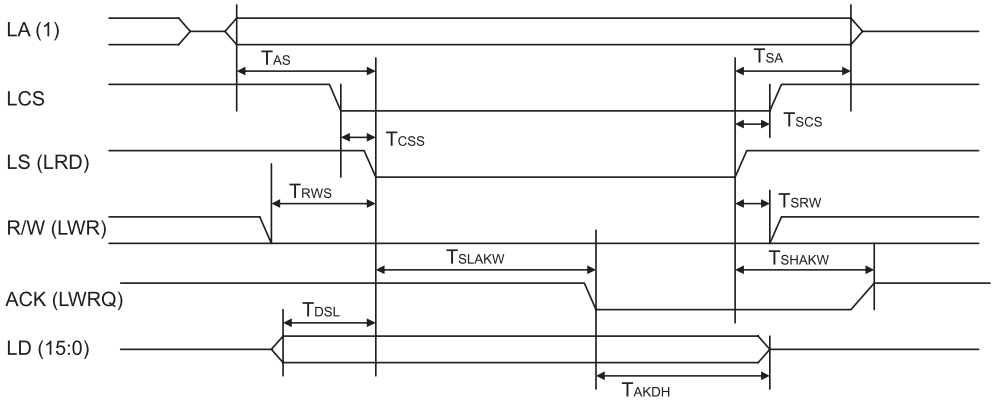
Note1: When CKSL = LOW or CKSL = HIGH, the data output delay time will be 12 T_{CLK} + 11.
Note 2: The time that the WRQ signal is output will be the interval after WRQ goes HIGH until WR goes HIGH.

11-5-4. 16-bit I/F (2) (IF1 = L, IF0 = L)

- Read cycle



- Write cycle



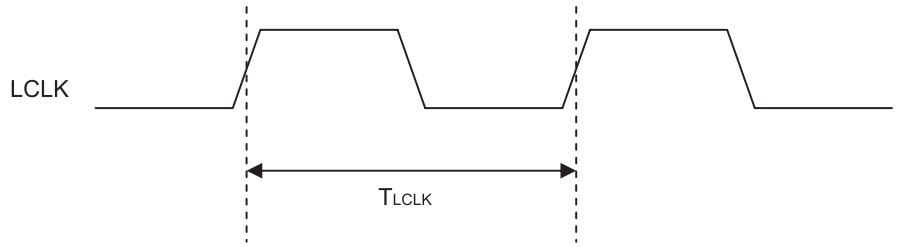
Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LS ↓	T_{As}		17		ns
Address hold time for LS ↑	T_{sa}		0		ns
LCS setup time for LS ↓	T_{css}		8		ns
LCS hold time for LS ↑	T_{scs}		0		ns
R/W setup time for LS ↓	T_{RWS}		3		ns
R/W hold time for LS ↑	T_{SRW}		4		ns
ACK=ON delay time for LS ↓	T_{SLAKR}	C_L = 40pF Note 1	$2T_{CLK}$	$6T_{CLK}$+9	ns
	T_{SLAKW}	C_L = 40pF Note 1	$2T_{CLK}$	$6T_{CLK}$+9	ns
ACK=ON delay time for LS ↑	T_{SHAKR}	C_L = 40pF		16	ns
	T_{SHAKW}	C_L = 40pF		16	ns
Data float delay time for ACK ↓	T_{DAKLR}	C_L = 40pF Note 2	$2T_{CLK}$		ns
Data float delay time for LS ↑	T_{SHD}	C_L = 40pF		30	ns
Data setup time for LS ↑	T_{DSL}		22		ns
Data hold time for ACK↓	T_{AKDH}		0		ns

Note 1: When CKSL = LOW or CKSL = HIGH, MIN = $4T_{CLK}$ and MAX = $12T_{CLK}$+9.
Note 2: When CKSL = LOW or CKSL = HIGH, MIN = $4T_{CLK}$.

11-6. Timing when CPU emulation is selected

11-6-1. LCLK timing

The LCLK uses the following timing, even when the device is not in the emulation mode



- When CKSL = L (400 MHz, T_{CLK} = 25 ns)

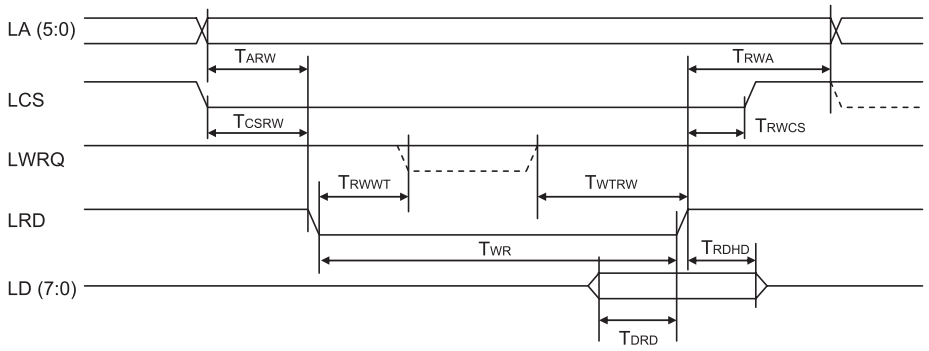
Item	Symbol	Condition	Cycle	Unit
Clock cycle	T_{LCLK}	LCK1 = L, LCK0 = L 2 MHz	$20T_{CLK}$	ns
		LCK1 = L, LCK0 = H 4 MHz	$10T_{CLK}$	
		LCK1 = H, LCK0 = L 10MHz	$4T_{CLK}$	
		LCK1 = H, LCK0 = H 20 MHz	$2T_{CLK}$	

- When CKSL = H (80 MHz, T_{CLK} = 25 ns)

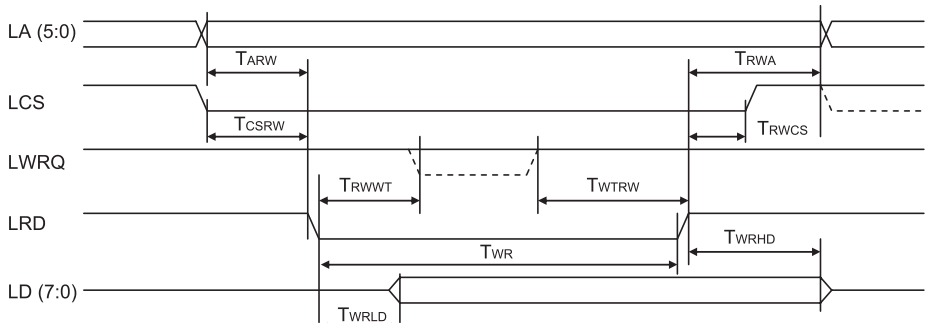
Item	Symbol	Condition	Cycle	Unit
Clock cycle	T_{LCLK}	LCK1 = L, LCK0 = L 2 MHz	$40T_{CLK}$	ns
		LCK1 = L, LCK0 = H 4 MHz	$20T_{CLK}$	
		LCK1 = H, LCK0 = L 10MHz	$8T_{CLK}$	
		LCK1 = H, LCK0 = H 20 MHz	$4T_{CLK}$	

11-6-2. 8-bit I/F (1) (IF1 = H, IF0 = H)

- Read cycle



- Write cycle

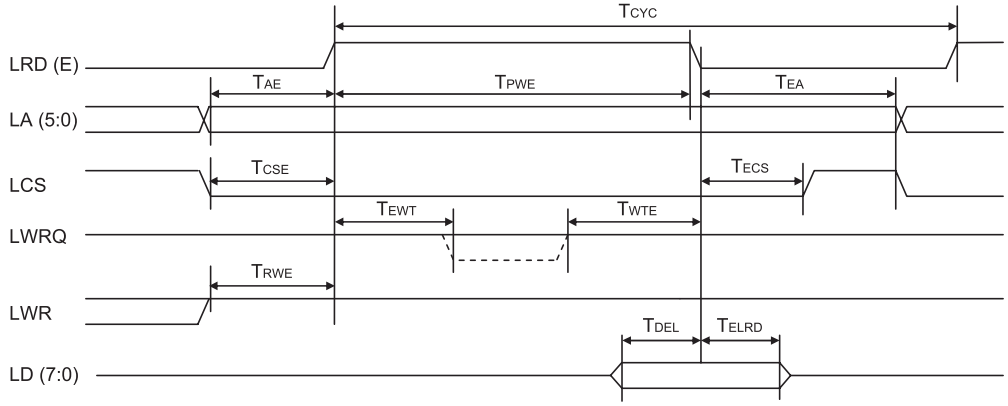


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LRD, LWR ↓	T_{ARW}		T_{LCLK} -1	T_{LCLK} +1	ns
Address hold time for LRD, LWR ↑	T_{RWA}	LWT1 = L, LWT0 = L Note	T_{LCLK} -1	T_{LCLK} +1	ns
CS setup time for LRD, LWR ↓	T_{CSRW}		T_{LCLK} -1	T_{LCLK} +1	ns
CS hold time for LRD, LWR ↑	T_{RWCS}		0	1	ns
LWRQ=ON set up time for LRD, LWR ↓	T_{RWWT}			T_{LCLK} -12	ns
LRD, LWR = OFF signal LOW time for LWRQ ↑	T_{WTRW}	CL = 40pF	$2T_{LCLK}$ +2	$3T_{LCLK}$	ns
Data setup time for LRD ↑	T_{DRD}		23		ns
Data hold time for LRD ↑	T_{RDHD}		0		ns
LRD signal width	T_{RD}		$2T_{LCLK}$		ns
LWR signal width	T_{WR}		$2T_{LCLK}$		ns
Data output delay time for LWR ↓	T_{WRLD}	CL = 40pF	5	15	ns
Data hold time for LWR ↑	T_{WRHD}		T_{LCLK} -2	T_{LCLK} +1	ns

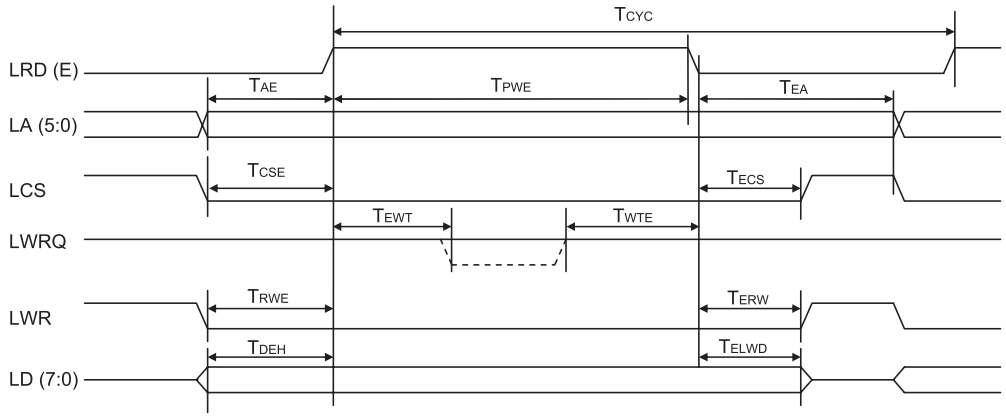
Note: The addresses do not change until the next cycle, so the hold time varies with value used for LWT.

11-6-3. 8-bit I/F (2) (IF1 = H, IF0 = L)

- Read cycle



- Write cycle

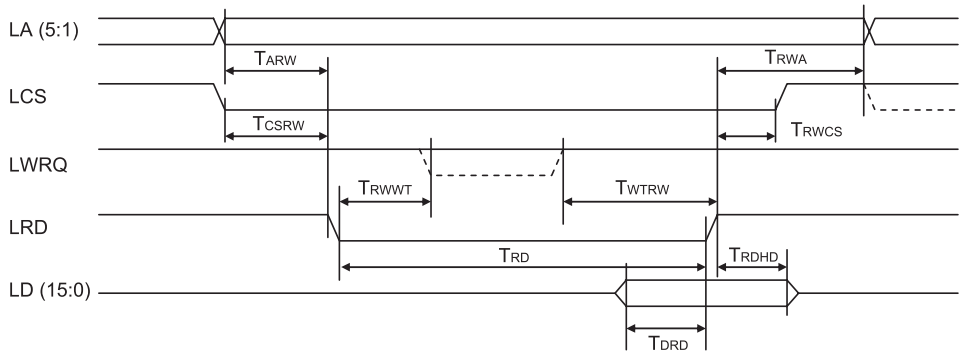


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LRD (E) ↑	T_{AE}		T_{LCLK} -1	T_{LCLK} +1	ns
Address hold time for LRD (E) ↓	T_{EA}	LWT1 = L, LWT0 = L Note	$2T_{LCLK}$ -1	$2T_{LCLK}$ +1	ns
R/W setup time for LRD (E) ↑	T_{RWE}		T_{LCLK} -1	T_{LCLK} +1	ns
R/W hold time for LRD (E) ↓	T_{ERW}		T_{LCLK} -1	T_{LCLK} +1	ns
LCS setup time for LRD (E) ↑	T_{CSE}		T_{LCLK} -1	T_{LCLK} +1	ns
LCS hold time for LRD (E) ↓	T_{ECS}		T_{LCLK} -1	T_{LCLK} +1	ns
LWRQ=ON set time for LRD (E) ↑	T_{EWT}	CL = 40pF		$2T_{LCLK}$ -12	ns
LWRQ signal LOW time for LWRQ ↑	T_{WTE}	CL = 40pF	T_{LCLK} +2	$2T_{LCLK}$	ns
Data setup time for LRD (E) ↓	T_{DEL}		23		ns
Data hold time for LRD (E) ↓	T_{ELRD}		0		ns
LRD (E) signal width	T_{PWE}		$2T_{LCLK}$		ns
LRD (E) cycle time	T_{CYC}		$5T_{LCLK}$		ns
Data setup time for LRD (E) ↓	T_{DEL}		T_{LCLK} -3	T_{LCLK} +1	ns
Data hold time for LRD (E) ↓	T_{ELDW}		T_{LCLK} -1	T_{LCLK} +1	ns

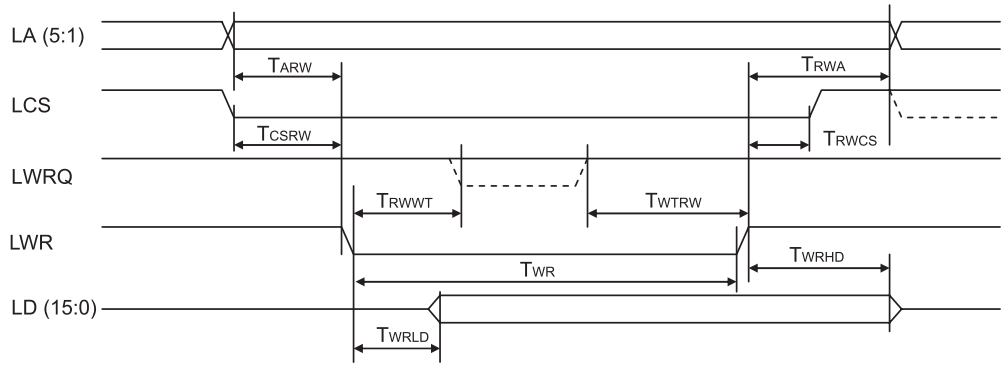
Note 1: When CKSL = LOW or CKSL = HIGH, the data output delay time will be 12 T_{CLK} + 11.

11-6-4. 16-bit I/F (1) (IF1 = L, IF0 = H)

- Read cycle



- Write cycle

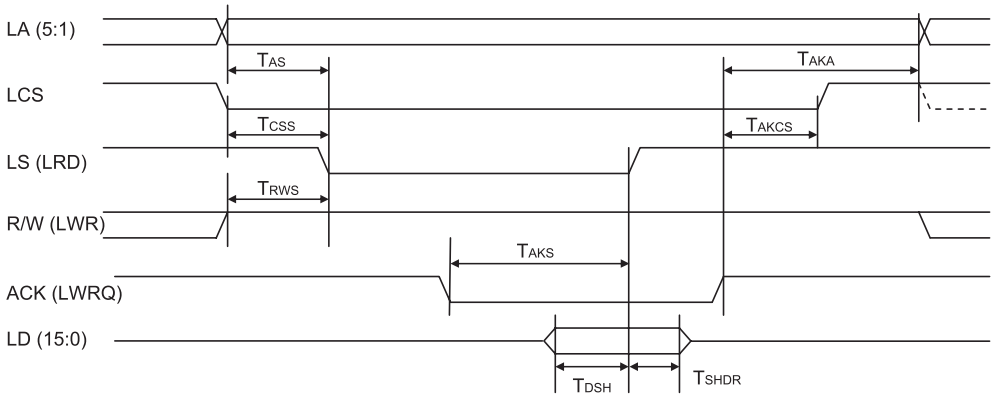


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LRD, LWR ↓	T_{ARW}		T_{LCLK} -1	T_{LCLK} +1	ns
Address hold time for LRD, LWR ↑	T_{RWA}	LWT1 = L, LWT0 = L Note	T_{LCLK} -1	T_{LCLK} +1	ns
CS setup time for LRD, LWR ↓	T_{CSRW}		T_{LCLK} -1	T_{LCLK} +1	ns
CS hold time for LRD, LWR ↑	T_{RWCS}		0	1	ns
LWRQ=ON set time for LRD, LWR ↓	T_{RWWT}			T_{LCLK} -12	ns
LRD, LWR = OFF delay time for LWRQ ↑	T_{WTRW}	CL = 40pF	$2T_{LCLK}$ +2	$3T_{LCLK}$	ns
Data setup time for LRD ↑	T_{DRD}		23		ns
Data hold time for LRD ↑	T_{RDHD}		0		ns
LWR signal width	T_{RD}		$2T_{LCLK}$		ns
LWR cycle time	T_{WR}		$2T_{LCLK}$		ns
Data setup time for LWR ↓	T_{WRLD}	CL = 40pF	5	15	ns
Data hold time for LWR ↑	T_{WRHD}		T_{LCLK} -2	T_{LCLK} +1	ns

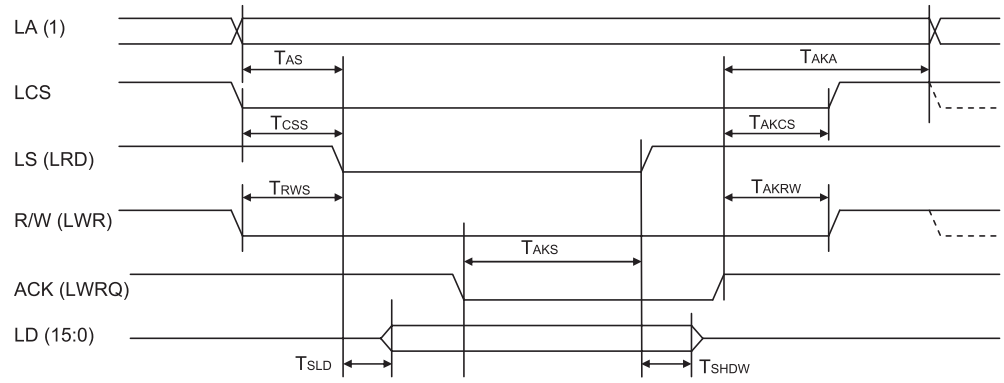
Note: The hold time varies with the LWT set value as the address does not change until next cycle.

11-6-5. 16-bit I/F (2) (IF1 = L, IF0 = L)

- Read cycle



- Write cycle

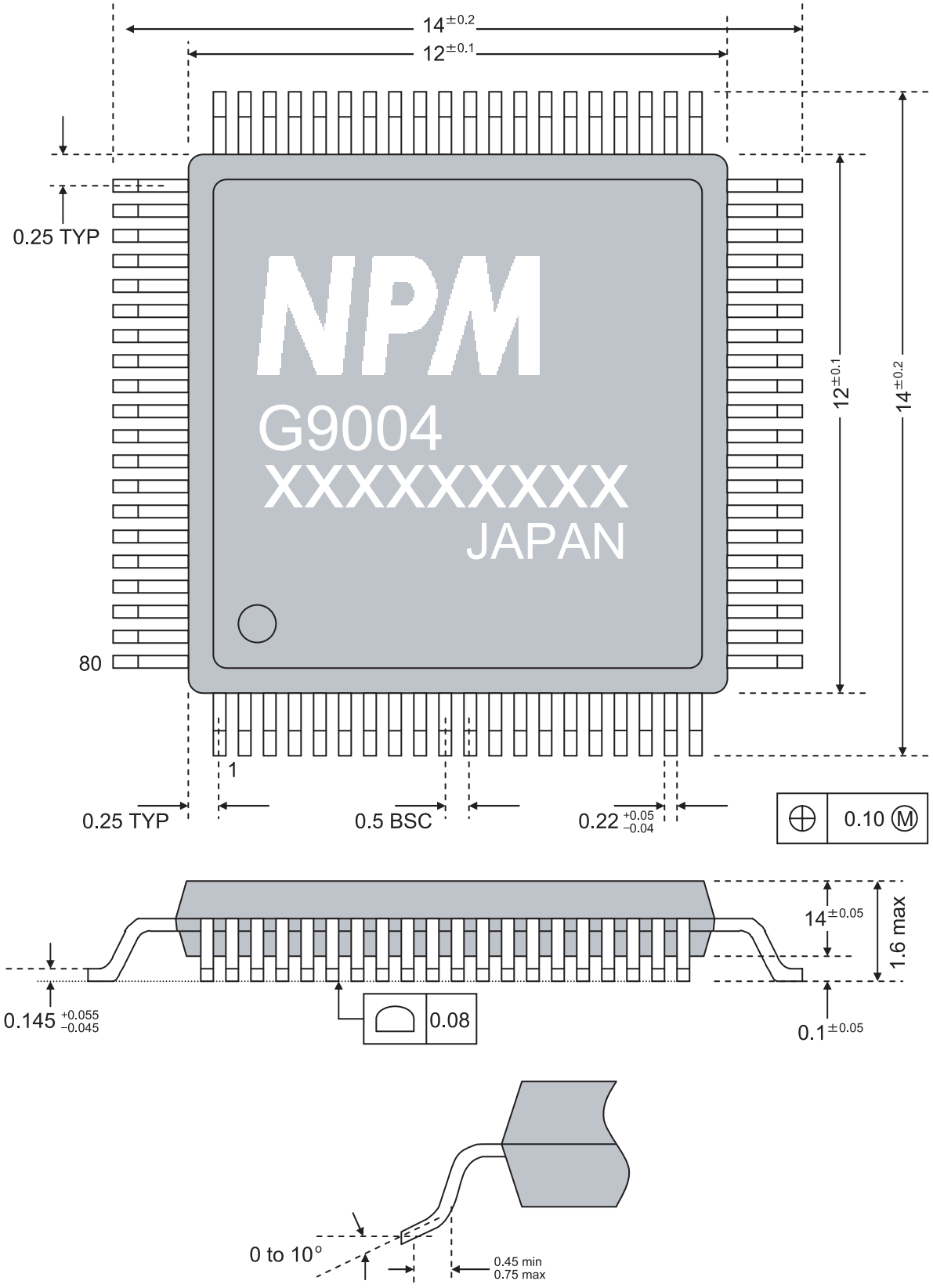


Item	Symbol	Condition	Min.	Max.	Unit
Address setup time for LS ↓	T_{AS}		T_{LCLK} -1	T_{LCLK} +1	ns
Address hold time for ACK ↑	T_{AKA}	LWT1 = L, LWT0 = L Note	$2T_{LCLK}$ -1	$3T_{LCLK}$ +1	ns
LCS setup time for LS ↓	T_{CSS}		T_{LCLK} -1	T_{LCLK} +1	ns
LCS hold time for ACK ↑	T_{AKCS}		T_{LCLK} -1	$2T_{LCLK}$ +1	ns
R/W setup time for LS ↓	T_{RWS}		T_{LCLK} -1	T_{LCLK} +1	ns
R/W hold time for ACK ↑	T_{AKRW}		T_{LCLK} -1	$2T_{LCLK}$ +1	ns
LS (LRD) OFF delay time for ACK ↓	T_{AKS}	CL= 40pF	T_{LCLK}	$2T_{LCLK}$ +1	ns
Data setup time for LS ↑	T_{DSH}		23		ns
Data hold time for LS ↑	T_{SHDR}		0		ns
Data output delay time for LS ↓	T_{SLD}	CL= 40pF	2	17	ns
Data hold time for LS ↑	T_{SHDW}		0	1	ns

Note: The hold time varies with the LWT set value as the address does not change until next cycle.

12. External dimensions

80pin LQFP Unit: mm



13. Handling precautions

13-1. Design precautions

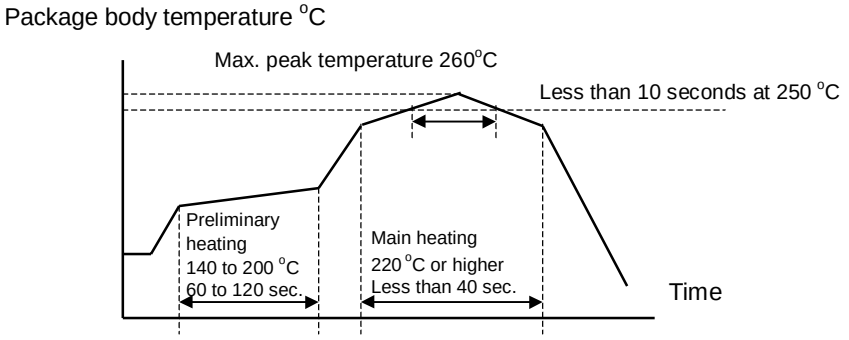
1) Never exceed the absolute maximum ratings, even for a very short time.
2) Take precautions against the influence of heat in the environment, and keep the temperature around the LSI as cool as possible.
3) Please note that ignoring the following may result in latching up and may cause overheating and smoke.
   - Do not apply a voltage greater than +3.3V (greater than 5V for 5V connectable terminals) to the input/output terminals and do not pull them below GND.
   - Please consider the voltage drop timing when turning the power ON/OFF. Consider power voltage drop timing when turning ON/OFF the power.
   - Make sure you consider the input timing when power is applied.
   - Be careful not to introduce external noise into the LSI.
   - Hold the unused input terminals to +3.3 V or GND level.
   - Do not short-circuit the outputs.
   - Protect the LSI from inductive pulses caused by electrical sources that generate large voltage surges, and take appropriate precautions against static electricity.
4) Provide external circuit protection components so that overvoltages caused by noise, voltage surges, or static electricity are not fed to the LSI.

13-2. Precautions for transporting and storing LSIs

1) Always handle LSIs carefully and keep them in their packages. Throwing or dropping LSIs may damage them.
2) Do not store LSIs in a location exposed to water droplets or direct sunlight.
3) Do not store the LSI in a location where corrosive gases are present, or in excessively dusty environments.
4) Store the LSIs in an anti-static storage container, and make sure that no physical load is placed on the LSIs.

13-3. Precautions for mounting

1) Plastic packages absorb moisture easily. Even if they are stored indoors, they will absorb moisture as time passes. Putting the packages in to a solder reflow furnace while they contain moisture may cause cracks in plastic case or deteriorate the bonding between the plastic case and the frame.
   The storage warranty period is one year as long as the moisture barrier bags are not opened.
2) If you are worried about moisture absorption, dry the chip packages thoroughly before reflowing the solder.
   Dry the packages for 20 to 36 hours at 125+/-5^{o}C. The packages should not be dried more than two times.
3) To heat the entire package for soldering, such as infrared or superheated air reflow, make sure to observe the following conditions and do not reflow more than two times.
   - Temperature profile
     The temperature profile of an infrared reflow furnace must be within the range shown in the figure below. (The temperatures shown are the temperature at the surface of the plastic package.)
   - Maximum temperature
     The maximum allowable temperature at the surface of the plastic package is 260^{o}C peak [A profile]. The temperature must not exceed 250^{o}C [A profile] for more than 10 seconds. In order to decrease the heat stress load on the packages, keep the temperature as low as possible and as short as possible, while maintaining the proper conditions for soldering.



[A profile (applied to lead-free soldering)]

4) Solder dipping causes rapid temperature changes in the packages and may damage the devices. Therefore, do not use this method.

13-4. Other precautions

1) When the LSI will be used in poor environments (high humidity, corrosive gases, or excessive amounts of dust), we recommend applying a moisture prevention coating.
2) The package resin is made of fire-retardant material; however, it can burn. When baked or burned, it may generate gases or fire. Do not use it near ignition sources or flammable objects.
3) This LSI is designed for use in commercial apparatus (office machines, communication equipment, measuring equipment, and household appliances). If you use it in any device that may require high quality and reliability, or where faults or malfunctions may directly affect human survival or injure humans, such as in nuclear power control devices, aviation devices or spacecraft, traffic signals, fire control, or various types of safety devices, we will not be liable for any problem that occurs, even if it was directly caused by the LSI. Customers must provide their own safety measures to ensure appropriate performance in all circumstances.

Notes

NPM NIPPON PULSE MOTOR CO., LTD.

Tokyo Office: No. 16-13, 2-chome, Hongo, Bunkyo-ku, Tokyo 113-0033, Japan
Phone: 81-3-3813-8841 Fax: 81-3-3813-7049
E-mail: device@npm.co.jp http://www.pulsemotor.com

NIPPON PULSE AMERICA, INC.: 1073 East Main Street, Radford, VA 24141, U.S.A.
Phone: 1-540-633-1677 Fax: 1-540-633-1674
E-mail: info@nipponpulse.com http://www.nipponpulse.com

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